RCA Solid State

QMOS

RCA High-speed CMOS Logic

# DATABOOK

# QMOS High-Speed CMOS Logic ICs

# RCA QMOS Integrated Circuits

QMOS
High-speed CMOS Logic

The RCA QMOS series of high-speed CMOS logic integrated circuits include an extensive line of products that are pin compatible with many existing bipolar 54/74 LSTTL and CMOS 4000 series of digital logic types. The new QMOS IC's provide high-speed CMOS replacements for the most popular LSTTL devices in existing designs and also offer low-power all-CMOS designs for new digital systems. Key family features of the RCA QMOS types include:

- Speeds equivalent to LSTTL types with typical gate delays of 8 ns.
- Fanout to 10 74 LSTTL loads; 15 loads using Bus Driver 54/74 types.
- Operating frequencies equivalent to LSTTL types, typically 50 MHz.
- The high voltage noise immunity characteristic of CMOS, typically 45 percent of $V_{CC}$, a two to three times improvement over LSTTL. (HC-Series types.)
- Wide range of power supply operating voltages, 2 to 6 volts.
- CMOS low static power consumption, typically less than 1 microwatt.

With the broad line of CMOS MSI function types currently available, together with performance offered by the RCA QMOS series of high-speed CMOS integrated circuits, the designer need not sacrifice speed for power consumption. Add the other classical advantages of CMOS, including high noise immunity and wide power supply and temperature ranges, and the decision to use high-speed CMOS logic (QMOS) is the choice for the 80's. This new family provides for the design of more cost-effective systems to serve high-speed market applications.

The RCA QMOS product line consists of CD54/74HC-series types, which feature CMOS input voltage level compatibility and CD54/74HCT-series types, which are input voltage level compatible with LSTTL devices. The QMOS line also includes a limited number of single-stage, unbuffered inverter types (CD54/74HCU-series) for added versatility in oscillator and amplifier applications.

The data pages include a description, special features, truth tables and/or timing diagrams, and significant dynamic electrical characteristics.

A general information section defines the distinguishing characteristics of each product series and provides characteristic data and classification and selection charts.

The data sections are followed by a Dimensional Outlines section.

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The device data shown for some types are indicated as preliminary. **Preliminary data** are intended for guidance purposes in evaluating devices for equipment design. Such data are shown for types currently being designed for inclusion in our standard line of commercially available products. For current information on the status of Preliminary devices described, please contact your local RCA sales office.

When incorporating RCA Solid State Devices in equipment, it is reccommended that the designer refer to "Operating Considerations for RCA Solid State Devices," Form No. ICE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.



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# Product Selector

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Note: Add package suffix code to part number on all orders.
E = Dual-In-Line Plastic Package—Temp. Range = -40°C to +85°C.
F = Dual-In-Line Frit-Seal Ceramic Package (CERDIP)—Temp. Range = -55°C to +125°C.

**Typical Dual-In-Line Plastic Package**

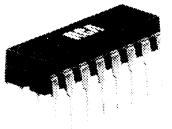

**Fig. 1—Dual-in-line plastic package**

**Typical Dual-In-Line Frit-Seal Ceramic Package**

**Fig. 2—Dual-in-line Frit-seal ceramic (CERDIP) package**

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| HC/HCT40104* | 4-Bit Bidirectional Universal Shift Register; 3-State | MSI | 159 |
| | **Arithmetic Circuits** | | |
| HC/HCT85 | 4-Bit Magnitude Comparator | MSI | 117 |
| HC/HCT384 | 8-Bit Serial/Parallel Two's Complement Multiplier | MSI | 140 |
| HC/HCT688 | 8-Bit Magnitude Comparator | MSI | 147 |

*Types with a bus driver output stage.

# QMOS Product Selection Guide (Cont'd)

| Type | Function/Description | Classification | Page |
|---|---|---|---|
| **CD54/74** | **Counters** | | |
| HC/HCT160 | Presettable Synchronous BCD Decade Counter; Asynchronous Reset | MSI | 125 |
| HC/HCT161 | Presettable Synchronous 4-Bit Binary Counter; Asynchronous Reset | MSI | 125 |
| HC/HCT162 | Presettable Synchronous BCD Decade Counter; Synchronous Reset | MSI | 125 |
| HC/HCT163 | Presettable Synchronous 4-Bit Binary Counter; Synchronous Reset | MSI | 125 |
| HC/HCT190 | Presettable Synchronous BCD Decade Up/Down Counter | MSI | 128 |
| HC/HCT191 | Presettable Synchronous 4-Bit Binary Up/Down Counter | MSI | 128 |
| HC/HCT192 | Presettable Synchronous BCD Decade Up/Down Counter | MSI | 129 |
| HC/HCT193 | Presettable Synchronous 4-Bit Binary Up/Down Counter | MSI | 129 |
| HC/HCT390 | Dual Decade Ripple Counter | MSI | 141 |
| HC/HCT393 | Dual 4-Bit Binary Ripple Counter | MSI | 141 |
| HC/HCT4017 | Johnson Decade Counter with 10 Decoded Outputs | MSI | 149 |
| HC/HCT4020 | 14-Stage Binary Ripple Counter | MSI | 101 |
| HC/HCT4024 | 7-Stage Binary Ripple Counter | MSI | 149 |
| HC/HCT4040 | 12-Stage Binary Ripple Counter | MSI | 106 |
| HC/HCT4060 | 14-Stage Binary Ripple Counter with Oscillator | MSI | 152 |
| HC/HCT4518 | Dual Synchronous BCD Counter | MSI | 156 |
| HC/HCT4520 | Dual 4-Bit Synchronous Binary Counter | MSI | 156 |
| HC/HCT40102 | 8-Bit Synchronous BCD Down Counter | MSI | 158 |
| HC/HCT40103 | 8-Bit Binary Down Counter | MSI | 158 |
| | **Multiplexers** | | |
| HC/HCT151 | 8-Input Multiplexer | MSI | 122 |
| HC/HCT153 | Dual 4-Input Multiplexer | MSI | 123 |
| MC/HCT157 | Quad 2-Input Multiplexer | MSI | 124 |
| HC/HCT158 | Quad 2-Input Multiplexer; Inverting | MSI | 55 |
| HC/HCT251 | 8-Input Multiplexer; 3-State | MSI | 80 |
| HC/HCT253 | Dual 4-Input Multiplexer; 3-State | MSI | 132 |
| HC/HCT257* | Quad 2-Input Multiplexer; 3-State | MSI | 133 |
| HC/HCT354* | 8-Input Multiplexer/Register; 3-State | MSI | 135 |
| HC/HCT356* | 8-Input Multiplexer/Register; 3-State | MSI | 135 |
| | **Decoders/Encoders** | | |
| HC/HCT42 | BCD to Decimal Decoder (1-of-10) | MSI | 116 |
| HC/HCT138 | 3-to-8-Line Decoder/Demultiplexer; Inverting | MSI | 50 |
| HC/HCT139 | Dual 2-to-4-Line Decoder/Demultiplexer | MSI | 121 |
| HC/HCT147 | 10-to-4-Line Priority Encoder | MSI | 122 |
| HC/HCT154 | 4-to-16-Line Decoder/Demultiplexer | MSI | 123 |
| HC/HCT238 | 3-to-8-Line Decoder/Demultiplexer | MSI | 50 |
| HC/HCT280 | 9-Bit Odd/Even Parity Generator/Checker | MSI | 134 |
| HC/HCT4511 | BCD-to-7-Segment Latch/Decoder/Driver | MSI | 154 |
| HC/HCT4514 | 4-to-16-Line Decoder/Demultiplexer with Input Latches | MSI | 155 |
| HC/HCT4515 | 4-to-16-Line Decoder/Demultiplexer with Input Latches | MSI | 155 |
| HC/HCT4543 | BCD-to-7-Segment Latch/Decoder/Driver for LCDs | MSI | 157 |
| | **Switches** | | |
| HC/HCT4016 | Quad Bilateral Switch | SSI | 148 |
| HC/HCT4051 | 8-Channel Analog Multiplexer/Demultiplexer | MSI | 151 |
| HC/HCT4052 | Dual 4-Channel Analog Multiplexer/Demultiplexer | MSI | 151 |
| HC/HCT4053 | Triple 2-Channel Analog Multiplexer/Demultiplexer | MSI | 151 |
| HC/HCT4066 | Quad Bilateral Switch | SSI | 148 |
| HC/HCT4067 | 16-Channel Analog Multiplexer/Demultiplexer | MSI | 152 |
| | **Bus Transceivers** | | |
| HC/HCT242* | Quad Bus Transceiver; 3-State; Inverting | MSI | 75 |
| HC/HCT243* | Quad Bus Transceiver; 3-State | MSI | 75 |
| HC/HCT245* | Octal Bus Transceiver; 3-State | MSI | 132 |
| HC/HCT640* | Octal Bus Transceiver; 3-State; Inverting | MSI | 144 |
| HC/HCT643* | Octal Bus Transceiver; 3-State; True/Inverting | MSI | 144 |
| HC/HCT646* | Octal Bus Transceiver/Register; 3-State | MSI | 145 |
| HC/HCT648* | Octal Bus Transceiver/Register; 3-State; Inverting | MSI | 145 |
| | **Schmitt Triggers** | | |
| HC/HCT14 | Hex Inverting Schmitt Trigger | SSI | 114 |
| HC/HCT132 | Quad 2-Input NAND Schmitt Trigger | SSI | 121 |
| | **One-Shot Multivibrators** | | |
| HC/HCT123 | Dual Retriggerable Monostable Multivibrator with Reset | MSI | 120 |
| HC/HCT221 | Dual Monostable Multivibrator with Reset | MSI | 120 |
| HC/HCT423 | Dual Retriggerable Monostable Multivibrator with Reset | MSI | 120 |
| HC/HCT4538 | Dual Retriggerable Precision Monostable Multivibrator | MSI | 156 |
| HC/HCT297 | Digital Phase-Locked-Loop Filter | MSI | 134 |
| HC/HCT4046 | Phase-Locked Loop with VCO | MSI | 150 |

*Types with a bus driver output stage.

## Cross-Reference Guide

| Generic Device Number | RCA | | Phillips/ Signetics | | Motorola | | National | | Texas Instruments | |
|---|---|---|---|---|---|---|---|---|---|---|
| | HC | HCT | HC | HCT | HC | HCT | HC | HCT | HC | HCT |
| 00 | • | • | • | • | • | • | • | • | • | |
| 02 | • | • | • | • | • | | • | | • | |
| 04 | • | • | • | • | • | • | • | • | • | |
| 08 | • | • | • | • | • | | • | | • | |
| 10 | • | • | • | • | • | | • | | • | |
| 11 | • | • | • | • | • | | • | | • | |
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| 74 | • | • | • | • | • | | • | | • | |
| 75 | • | • | • | • | • | | • | | • | |
| 85 | • | • | • | • | • | | • | | • | |
| 86 | • | • | • | • | • | | • | | • | |
| 107 | • | • | • | • | • | | • | | • | |
| 109 | • | • | • | • | • | | • | | • | |
| 112 | • | • | • | • | • | | • | | • | |
| 123 | • | • | • | • | • | | • | | • | |
| 132 | • | • | • | • | • | | • | | • | |
| 138 | • | • | • | • | • | • | • | • | • | |
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| 153 | • | • | • | • | • | | • | | • | |
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| 163 | • | • | • | • | • | | • | | • | |
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| 165 | • | • | • | • | • | | • | | • | |
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| 259 | • | • | • | • | • | | • | | • | |
| 273 | • | • | • | • | • | | • | | • | |
| 280 | • | • | • | • | • | | • | | • | |
| 297 | • | • | • | • | | | | | | |

## Cross-Reference Guide

| Generic Device Number | RCA | | Phillips/ Signetics | | Motorola | | National | | Texas Instruments | |
|---|---|---|---|---|---|---|---|---|---|---|
| | HC | HCT | HC | HCT | HC | HCT | HC | HCT | HC | HCT |
| 299 | • | • | • | • | • | | • | | • | |
| 354 | • | • | • | • | • | | • | | • | |
| 356 | • | • | • | • | • | | • | | • | |
| 365 | • | • | • | • | • | | • | | • | |
| 366 | • | • | • | • | • | | • | | • | |
| 367 | • | • | • | • | • | | • | | • | |
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| 373 | • | • | • | • | • | • | • | • | • | |
| 374 | • | • | • | • | • | • | • | • | • | |
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| 540 | • | • | • | • | • | | • | | | |
| 541 | • | • | • | • | • | | • | | | |
| 563 | • | • | • | • | • | | • | | • | |
| 564 | • | • | • | • | • | | • | | • | |
| 573 | • | • | • | • | • | | • | | • | |
| 574 | • | • | • | • | • | | • | | • | |
| 640 | • | • | • | • | • | • | • | • | • | |
| 643 | • | • | • | • | • | • | • | • | • | |
| 646 | • | • | • | • | • | | • | | • | |
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| 670 | • | • | • | • | | | | | | |
| 688 | • | • | • | • | • | • | • | | • | |
| 4002 | • | • | • | • | • | | • | | • | |
| 4015 | • | • | • | • | | | | | | |
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| 4040 | • | • | • | • | • | | • | | • | |
| 4046 | • | • | • | • | • | | • | | | |
| 4049 | • | | • | | • | | • | | | |
| 4050 | • | | • | | • | | • | | | |
| 4051 | • | • | • | • | • | | • | | | |
| 4052 | • | • | • | • | • | | • | | | |
| 4053 | • | • | • | • | • | | • | | | |
| 4060 | • | • | • | • | • | | • | | • | |
| 4066 | • | • | • | • | • | | • | | | |
| 4067 | • | • | • | • | | | | | | |
| 4075 | • | • | • | • | • | | • | | • | |
| 4094 | • | • | • | • | | | | | | |
| 4511 | • | • | • | • | • | | • | | • | |
| 4514 | • | • | • | • | • | | • | | • | |
| 4515 | • | • | • | • | | | | | • | |
| 4518 | • | • | • | • | • | | • | | | |
| 4520 | • | • | • | • | • | | • | | | |
| 4538 | • | • | • | • | • | | • | | • | |
| 4543 | • | • | • | • | • | | • | | | |
| 40102 | • | • | • | • | | | | | | |
| 40103 | • | • | • | • | | | | | | |
| 40104 | • | • | • | • | | | | | | |
| 40105 | • | • | • | • | | | | | | |

QMOS
High-speed CMOS Logic

# Description of QMOS Product Line

# QMOS Family Description

The RCA QMOS series of high-speed CMOS integrated circuits includes a functionally complete set of LSTTL equivalent types and selected equivalent CMOS CD4000-series types. The CD4000-series types selected are unique to CMOS families because of the versatility of the CMOS technology in relation to the bipolar technology. Each type will be offered in two versions:

1. CD54/74HCTXXXX-series types, which feature LSTTL input-voltage-level compatibility.
2. CD54/74HCXXXX-series types, which feature CMOS input-voltage-level compatibility.

A third version, CD54/74HCU, is an unbuffered type for linear or high-speed oscillation applications.

The QMOS family consists of a comprehensive set of buffers, transceivers, and registers that are popular in computer systems. A wide variety of popular logic, MUX's, encoders/decoders, counters, arithmetic units, multivibrators, display drivers, and phase-lock loops complete the family. Table I shows a breakdown of the QMOS Family by logic function:

**TABLE I — The QMOS Family**

| Device Type | Number of Functions |
|---|---|
| Inverters/Buffers/Bus Drivers | 13 |
| Flip-Flops/Latches/Registers | 22 |
| Bus Transceivers | 7 |
| Shift Registers | 9 |
| Counters | 18 |
| Decoders/Encoders | 11 |
| Multiplexers | 9 |
| Multivibrators | 4 |
| Gates/Schmitt Triggers | 13 |
| Phase-Lock Loops | 2 |
| Bilateral Switches | 6 |
| Arithmetic Circuits | 3 |

**QMOS Family Features**

- Function and pinning identical to the LSTTL and CD4000-series circuits.
- CMOS outputs for maximum noise margins.
- Fan-out (over temperature):
  Standard Outputs — 10 LSTTL loads
  Bus-Driver Outputs — 15 LSTTL loads
- Wide operating temperature range:
  CD74HC/HCT/HCU: −40 to +85°C
  CD54HC/HCT/HCU: −55 to +125°C
- Balanced propagation and transition times.
- Significant power reduction compared to LSTTL logic.
- Alternate source — Philips/Signetics

**Series Features**

CD54HCXXXX/CD74HCXXXX Series

- 2 to 6V operation.
- High noise immunity: $N_{IL}$ = 20%, $N_{IH}$ = 30% at $V_{CC}$ = 5V.

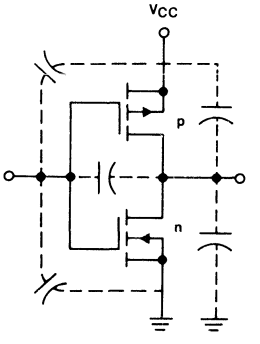
CD54HCTXXXX/CD74HCTXXXX Series

- 4.5 to 5.5V operation.
- Direct LSTTL input logic compabilitity
  $V_{IL}$ = 0.8V (max), $V_{IH}$ = 2.0V (min).
- CMOS input compatibility
  $I_{IL}$, $I_{IH} \leq 1\mu A$ at $V_{OL}$, $V_{OH}$

**Technology Overview**

The high speeds and low quiescent power dissipation that characterize the RCA QMOS family are made possible by utilizing a three-micron, self-aligned silicon-gate, CMOS process. The three-micron process minimizes the internal parasitic capacitances of the circuit, which results in increased switching speed.

The polysilicon gates of the transistors are deposited over a thin gate oxide before the source and drain diffusions are defined. Ion implantation is then used to form the source and drain areas, with the polysilicon gates acting as a mask for the implantation. The source and drain are automatically aligned to the gate, hence the expression "self-aligned-gate" process. In this manner, gate-to-source and gate-to-drain capacitances are minimized. Junction capacitances, which are proportional to the junction area, are also reduced because of the shallower diffusions. Figure 1 shows the parasitic capacitances present in a CMOS inverter.




92CS-37075

**Fig. 1—Parasitic capacitances in a CMOS inverter.**

In contrast, the source and drain areas in a metal-gate CMOS process are formed before the gate is deposited. Moreover, the metal gate must overlap the source and drain to allow for alignment tolerances. These conditions result in higher overlap capacitances than those present in QMOS devices. The metal-gate process also employs deeper diffusions than those in the QMOS process and, consequently, has larger junction capacitances.

The QMOS structure features a three-micron gate length; the CD4000-series structure has a gate length of seven microns. The equation for the drain current of a MOSFET is:

$$I_{DS} = K' \frac{\text{width}}{\text{length}} [(\text{gate voltage}) - (\text{threshold voltage})]^2$$

where K′ is the "beta" of the MOSFET. Therefore, a shorter gate length results in higher drive capability, which in turn increases the speed at which a transistor can charge or discharge capacitance.

The polysilicon in a silicon-gate process is also an interconnect layer; thus, there are three levels of interconnect (diffusion, polysilicon, and metal) instead of the two layers (diffusion and metal) present in a metal-gate process. This situation aids in making a more compact die. Figure 2 compares the cross sections of the seven-micron metal-gate CMOS structure and the three-micron silicon-gate QMOS structure.

### Input Characteristics

The inputs of QMOS devices are voltage-level sensitive, and do not require current, except for input leakage. The switching characteristics for the HC and HCT versions are illustrated in Figs. 3 and 4, respectively. These characteristics exhibit a very sharp transition that is very stable over the operating temperature range.

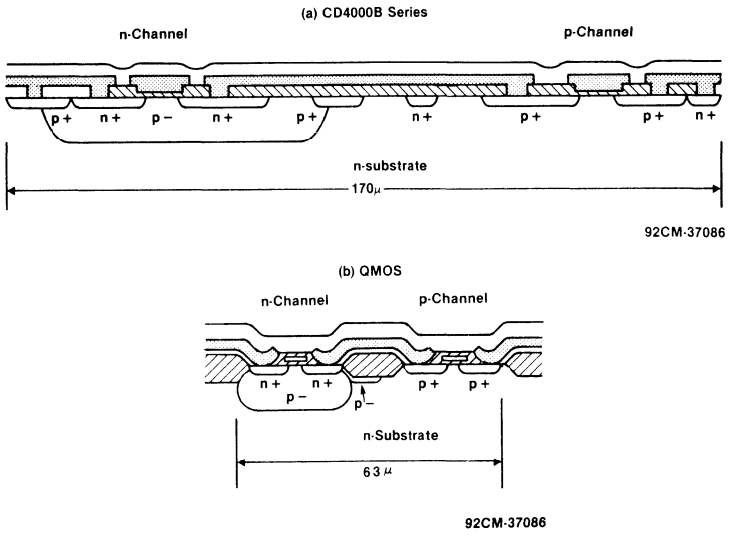



**Fig. 2.—Crossectional view of (a) the seven-micron CD4000B-Series structure and (b) three-micron QMOS structure.**

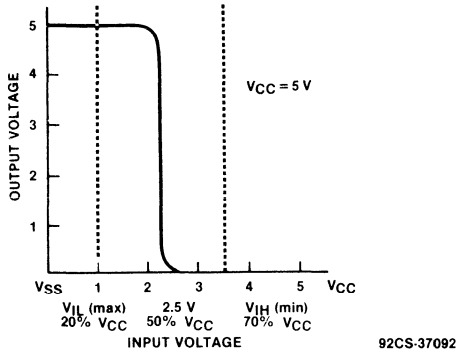



**Fig. 3—Switching characteristics of QMOS HC-series types.**

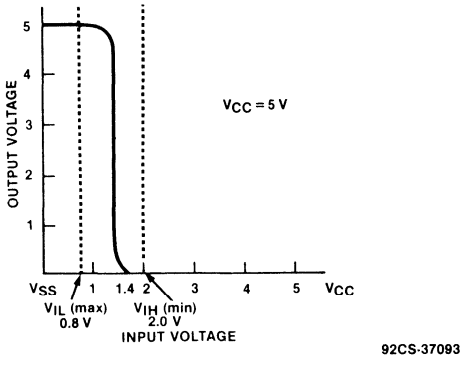



**Fig. 4—Switching characteristics of QMOS HCT-series types.**

The noise immunity, at $V_{CC} = 5V$, for all QMOS verions is highlighted in Table II.

**Table II—Noise Immunity at $V_{CC} = 5V$ for QMOS devices.**

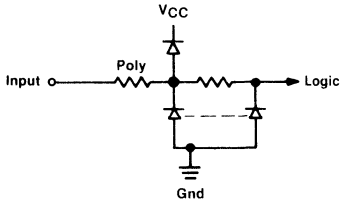
| | HC | HCT | HCU |
|---|---|---|---|
| $V_{IL}$ (max) | 1.0 | 0.8 | 1.0 |
| $V_{IH}$ | 3.5 | 2.0 | 4.0 |

The HC (with a few gate exceptions) and HCT types have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of the other inputs.

All unused inputs on a QMOS device must be terminated to $V_{CC}$ or ground. This practice is recommended when using TTL logic families to reduce power, but is sometimes not followed. Tying the unused inputs as noted avoids logic errors, unnecessary power consumption, and possible damage to the device.

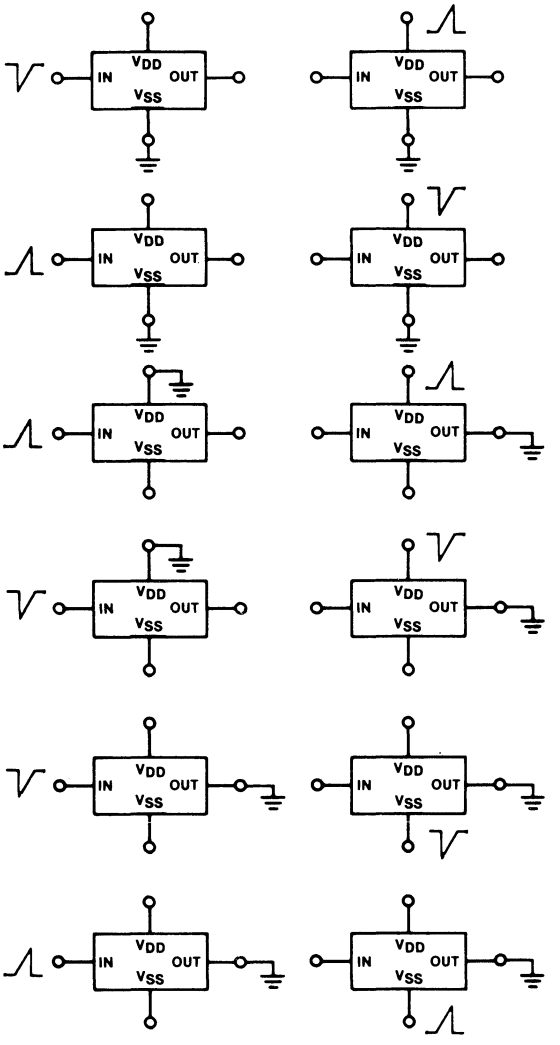
### Input Protection

QMOS device inputs have a resistor-diode protection network, shown in Fig. 5, that protects the gate oxide from electrostatic discharge (ESD) damage. The network provides protection to levels typically greater than 2kV in all modes pertaining to the input, as shown in Fig. 6. The 2kV figure was arrived at by testing devices in the ESD test circuit shown in Fig. 7 while conforming to the MIL-STD-38510 requirements. The recommended handling practices for QMOS devices are similar to those described in RCA Application Note ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."



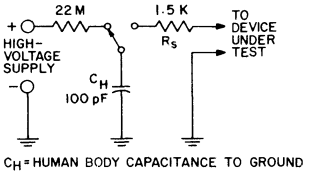

92CS-37083

**Fig. 5—Resistor-diode protection network used on inputs of QMOS devices to protect device gate oxide from electrostatic discharge damage.**




92CL-29324R1

**Fig. 6—QMOS input modes.**




$C_H$ = HUMAN BODY CAPACITANCE TO GROUND
$R_S$ = BODY SOURCE RESISTANCE

92CS-37074

**Fig. 7—Test circuit used to measure electrostatic discharge (ESD) resistance in QMOS circuits.**

### Input Currents

Both HC and HCT QMOS versions have ultra-low input currents, typically less than 10 pA. The input current is specified at ±1 μA for the full temperature range and results from the reverse leakages of the input-protection diodes. Note that the HCT version does not utilize any internal pull-up mechanisms at the input, and therefore both HC and HCT inputs present only a capacitive load, thus making fanout nearly infinite, as discussed below under the heading **Interfacing and Noise Margins.**

When the input voltage exceeds $V_{CC}$ or is below ground by greater than 500 mV, the input-protection diodes turn on and conduct current. The maximum input-current, $I_{IK}$, should not exceed ±20 mA. A resistor should be used in series with the input to limit the current to below ±20 mA if this input condition exists.

### Input Interaction

Another effect of the input-protection network is the imposition of a parasitic transistor between adjacent input pins. Fig. 8 shows this transistor.

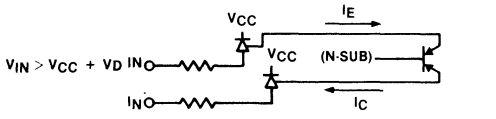



**Fig. 8—Parasitic transistor caused by input-protection network.**

This parasitic transistor may cause undesirable interaction between adjacent inputs if the input level is greater than $V_{CC}$ + $V_{diode}$. RCA QMOS devices minimize the alpha ($I_E/I_C$) to less than 0.05. This feature of the RCA QMOS inputs permits proper logic operation in the presence of most transients and also allows high-to-low voltage translation via series input resistors.

### Output Characteristics

QMOS outputs make use of a totem-pole CMOS configuration, which is different from the LSTTL output; both outputs are shown in Fig. 9. QMOS outputs meet the voltage-level requirements necessary to interface to CMOS inputs, and the drive and current requirements needed to interface to bipolar inputs; i.e., LS, ALS, FAST, etc.

The outputs of the QMOS devices are classified into two categories: standard and bus drive. The two outputs differ in the output transistor widths needed to meet drive and current requirements.

### Output Protection

The outputs in a QMOS device are protected from ESD damage by diodes. Figure 10 shows these diodes. Because of the large geometries (widths) of the output transistors, the inherent diodes are utilized. These diodes are the drain to n-substrate junction of the p device and the drain to p-well junction of the n device. This network provides protection to voltage levels typically greater than 3 kV in all modes pertaining to the output, Fig. 6.

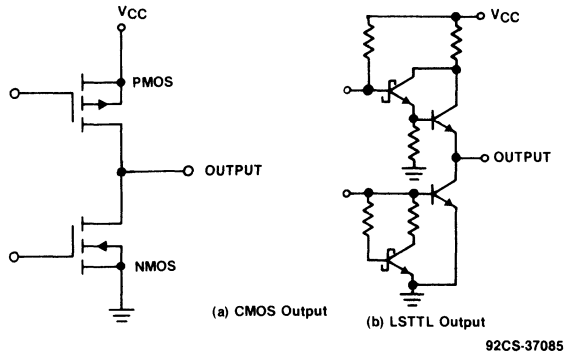



**Fig. 9—Comparison of QMOS (a) and LSTTL (b) outputs.**

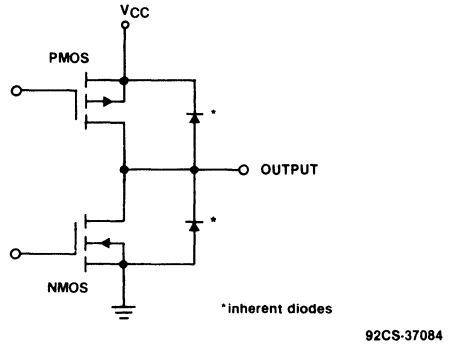



**Figure 10—Inherent diodes protecting QMOS output.**

### Output Currents

QMOS outputs are specified for both CMOS and LSTTL loads. Since CMOS inputs are voltage sensitive and the only current is leakage current, the specification is for $I_O$ = ±20 μA (20 CMOS loads). The outputs are also specified at $I_O$ = 4 mA (10 LSTTL loads) and 6 mA (15 LSTTL loads) for standard and bus-drive outputs, respectively. The corresponding $V_{OL}$(max) and $V_{OH}$(min) for the outputs, are illustrated in Table III.

**Table III—Output drive specifications.**

| Characteristic | Test Conditions/Limits | | | | UNIT |
|---|---|---|---|---|---|
| | $I_O$ | 25°C | -40/85°C | -55/125°C | |
| High-Level Output Voltage $V_{OH}$(min) | -20 μA | 4.4 | 4.4 | 4.4 | V |
| | -4mA | 3.98 | 3.84 | 3.7 | |
| | -6mA (Bus) | 3.98 | 3.84 | 3.7 | |
| Low-Level Output Voltage $V_{OL}$(max) | 20 μA | 0.1 | 0.1 | 0.1 | V |
| | 4mA | 0.26 | 0.33 | 0.4 | |
| | 6mA (Bus) | 0.26 | 0.33 | 0.4 | |

$V_{CC}$ = 4.5 V

The maximum current per output pin, $I_O$, is ±25 mA and ±35 mA for standard and bus-drive outputs, respectively. This maximum current rating is specified when the outputs are in their active regions: $-0.5V < V_O < V_{CC} + 0.5V$. The maximum current rating per power pin, $V_{CC}$ or ground, is 50 mA and 70 mA for standard or bus-drive, respectively.

When the output voltage exceeds $V_{CC}$ or is below ground by greater than 500 mV the output protection diodes turn on and conduct current. The maximum current, $I_{OK}$, should not exceed ±20 mA.

### Dynamic Characteristics

The RCA QMOS family is designed to meet the dynamic switching speeds and operating frequency of low-power Schottky TTL. When compared to metal-gate CD4000 and 74C series CMOS, QMOS shows a 10 to 1 improvement in ac performance. QMOS types feature balanced propagation delays and transition times specified for $V_{CC}$ = 4.5V and $C_L$ = 50 pF. Each QMOS data sheet will also specify the typical propagation delay at $V_{CC}$ = 5V and $C_L$ = 15 pF, so that the user can relate to the equivalent LSTTL specification. Test waveforms for the HC and HCT types are shown at the end of this section.

### Capacitive Load ($C_L$) Determination

The external capacitive loading ($C_L$) seen by a QMOS output is needed to calculate the propagation delay and operating power dissipation of a logic function. The three components of $C_L$ at a logic node are:

1. n $C_{IN}$ where n is the fan-out.
2. m $C_{OUT}$ where m is the number of three-state outputs on a logic bus.
3. $C_{STRAY}$ which is the effective wiring and interconnect capacitance.

$$C_L = n\,C_{IN} + (m - 1)C_{OUT} + C_{STRAY} \qquad (1)$$

$C_{IN}$ is shown in Fig. 11 for typical HCT and HC inputs. Note that $C_{IN}$ has peak values at the respective switch points of HCT (1.4V) and HC (2.5V). Capacitance on either side of the peak is a summation of package, lead-frame, reverse biased input diode, and CMOS gate-to-source/drain capacitance. The peak capacitance results from the Miller multiplication of C gate-to-drain in the high-gain linear-transition region. The values of $C_{IN}$ that most typically represent the average loading effect are 4 pF for HCT inputs and 3 pF for HC inputs. $C_{IN}$ for HCT inputs is higher than that for HC inputs because of the required large gate-to-source/drain capacitance of the large NMOS device widths.

Output capacitance ($C_{OUT}$) is typically 10 pF for both HCT and HC bus-driver outputs when these versions are in their high-Z state, the only state where $C_{OUT}$ loading is a factor.

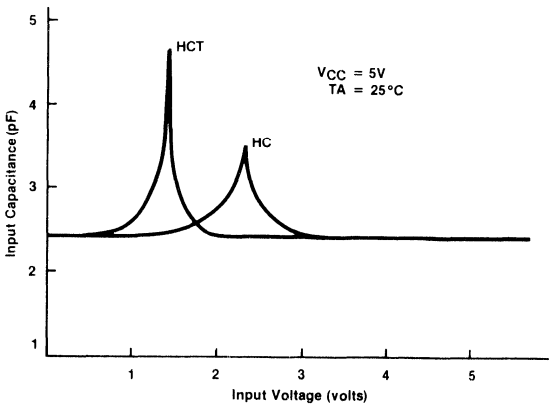



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**Fig. 11—$C_{IN}$ as a function of $V_{IN}$.**

The wiring and interconnect capacitance ($C_{STRAY}$) is determined by estimates of interconnect capacitance and wiring capacitance. These capacitances are highly variable because of differences in interwiring techniques. One often used high-speed wiring technique utilizes strip line with 100-ohm characteristic impedance. $C_{STRAY}$ in this case is typically 20 pF per foot. Capacitances of sockets and connectors are available from their manufacturers. In a bus system, $C_{STRAY}$ is the largest single $C_L$ component, as the following example illustrates:

*Bus Specification*
No. of fan-outs (n) = 10
No. of Bus Drivers (m) = 5
Length of Wiring = 7 ft.
From Equation (1):
$C_L = 10 \times 2.5\text{ pF} + 4 \times 10\text{ pF} + 7 \times 20\text{ pF}$
$= 25\text{ pF} + 40\text{ pF} + 140\text{ pF} = 205\text{ pF}$

Using the capacitive-loading propagation-delay loading factor for $C_L$, the bus-driver propagation delays are extended by .037 ns/pF or .037 ns x 205 pF = 7.58 ns.

### Propagation Delays

*Propagation delays versus Supply Voltage* — The dynamic performance of a CMOS device is related to its drain characteristics. The drain characteristics are related to the thresholds and gate-to-source voltage potential, $V_{gs}$. The $V_{gs}$ potential is equal to the power-supply potential, $V_{CC}$. Therefore, a reduction in $V_{CC}$ adversely affects the drain characteristics which, in turn increases the propagation delays. An increase in $V_{CC}$ decreases the propagation delays.

The HCT-version voltage range is 5V ± 10%. Over this range, the effects of propagation delays on performance

are minimal. However, the voltage range recommended for the HC-version is 2 to 6V. Over such a wide range, the effects on dynamic performance of propagation delay are appreciable. The typical dynamic characteristics for the HC version, normalized to 4.5V performance, are illustrated in Fig. 12.

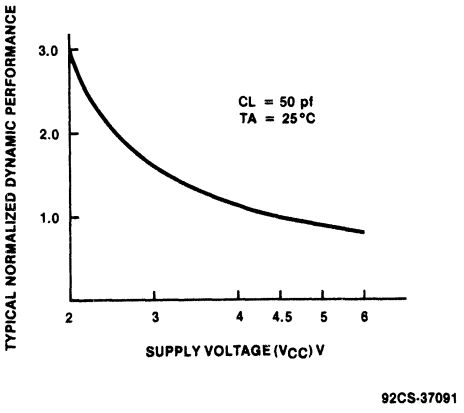



**Fig. 12—Typical dynamic characteristics versus supply voltage normalized to 4.5V dynamic characteristics.**

The typical propagation delay for any voltage can be calculated from the normalized dynamic performance by the following relationship:

$$t_{pd}(V) = tpd(4.5V) \times C \qquad (2)$$

where C = normalized delay at the voltage desired.

*Propagation Delay Versus Capacitance* — The dependence of propagation delay on capacitive loading in the QMOS technology has been reduced, in reference to CD4000 CMOS family, to a point where it is similar to that of LSTTL and ALS-series devices. The dependence, $t(C_L)$ at $V_{CC}$ = 4.5V, is typically 0.055 ns/pF and 0.037 ns/pF for standard and bus-drive outputs, respectively, as compared to a typical value of 1 ns/pF for the CD4000 series.

The propagation delay can, then, be computed for any load by using the following relationship:

$$tpd(C_L) = tpd(50\ pF) + t(C_L)[C_L - 50\ pF] \qquad (3)$$

*Propagation Delay Versus Temperature* — Since an increase in temperature causes a decrease in electron and hole mobilities, a temperature increase will cause an increase in QMOS propagation delays. Correspondingly, ac performance improves with lower temperatures. Typically, speeds derate linearly from 25°C at about −0.3%/°C.

Therefore, the propagation delay can be computed at any temperature between −55°C and +125°C by using the following relationship:

$$t_{pd}(T) = t_{pd}(25°C)\{1 + [(T(°C) - 25)(0.003\ (ns/°C)]\} \qquad (4)$$

**Output Transition Times**

Table IV shows the RCA standard and maximum ratings for output transition times applicable to all standard and bus-driver outputs. Typical values are approximately one half the maximum values. Practical unspecified minimum values are one fourth the limit values.

**Table IV—Output Transition Time Limits for $C_L$ = 50 pF**

| Output | $V_{CC}$ (V) | Maximum Output Transition Times (ns) | | |
|---|---|---|---|---|
| | | $T_A$ = 25°C | $T_A$ = 85°C | $T_A$ = 125°C |
| Standard | 2 | 75 | 95 | 110 |
| | 4.5* | 15 | 19 | 22 |
| | 6 | 13 | 16 | 19 |
| Bus Driver | 2 | 60 | 75 | 90 |
| | 4.5* | 12 | 15 | 18 |
| | 6 | 10 | 13 | 15 |

*Specification for CD54HCT and CD74HCT types.

**Power Supply Considerations**

*Power Supply Voltages* — The QMOS HC and HCU versions have a power-supply range of 2 to 6 V; the absolute-maximum voltage rating is 7 V. The ability to use QMOS HC types with a 2-V supply makes these devices particularly useful in battery-operated equipment, especially systems including memories that feature 2-V standby operation. The absolute-maximum supply or ground current, per pin, is ±50 mA for types with standard output drive, and ±70 mA for types with bus-driver outputs.

The operating supply range for QMOS CD74HCT types is 4.5 V to 5.5 V, 5 V ± 10%, while the supply range for 74LS types is 4.75 V to 5.25 V, 5 V ± 5%. These figures indicate that there is more tolerance in the regulation of the QMOS system supply than is the case with other technologies. The maximum voltage indicated for HC and HCU QMOS versions also applies to HCT versions. The advantages of using QMOS with its wider voltage supply range are illustrated in Fig. 13.

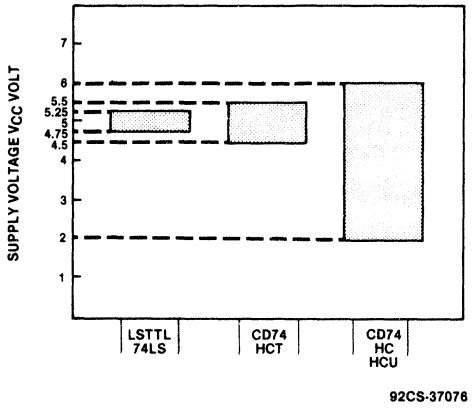



**Fig. 13—Power-supply ranges for 74LS, CD74HCT, CD74HC, and CD74HCU versions of the QMOS family of devices.**

*Power Consumption* — The power consumption of a QMOS device is composed of two components, one static, the other dynamic. The static component is the result of quiescent current, current caused by reverse junction leakage. The dynamic component results from transient currents required to charge and discharge the output capacitive load, transient currents caused by internal capacitance, and transients resulting from the overlapping of active p and n transistors. The latter two transients constitute a component represented by the value $C_{pd}$. Thus, the power consumption of a QMOS device is:

$$P = I_{CC}V_{CC} + C_{pd}V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o \quad (5)$$

where $I_{CC}$ = quiescent current
$V_{CC}$ = supply voltage
$f_i$ = input frequency
$f_o$ = output frequency
$C_{pd}$ = device equivalent capacitance load
$C_L$ = load capacitance

The specific method used to measure $C_{pd}$ is given in the Appendix.

The power consumption of an LSTTL device is also composed of a static and a dynamic component. LSTTL, because of its bipolar technology, requires higher static currents than those required by the CMOS technology. A comparison of the two technologies is given in Table V, which indicates the large quiescent (static) power differences between the LSTTL and QMOS technologies.

**Table V—QMOS and LSTTL Quiescent Current**

| Device Complexity | QMOS | | | | LSTTL |
|---|---|---|---|---|---|
| | Typical | 25°C | 85°C | 125°C | 125°C |
| SSI | 2 nA | 2 μA | 20 μA | 40 μA | 4.4 mA |
| FF | 4 nA | 4 μA | 40 μA | 80 μA | 8 mA |
| MSI | 8 nA | 8 μA | 80 μA | 160 μA | 10 mA/ 95 mA |

The dynamic power consumption of a QMOS device is frequency dependent, but it should be noted that LSTTL power consumption is also frequency dependent at frequencies greater than 1 MHz. At frequencies less than 1 MHz the dynamic component is negligible compared to the static component. The average power consumption of QMOS and LSTTL equivalents is illustrated in Fig. 14 for four device types. Since all of the functions in a multifunctional LSTTL device are biased when power is applied, the QMOS device characteristics are plotted for a single function and for the total package for the purposes of comparison.

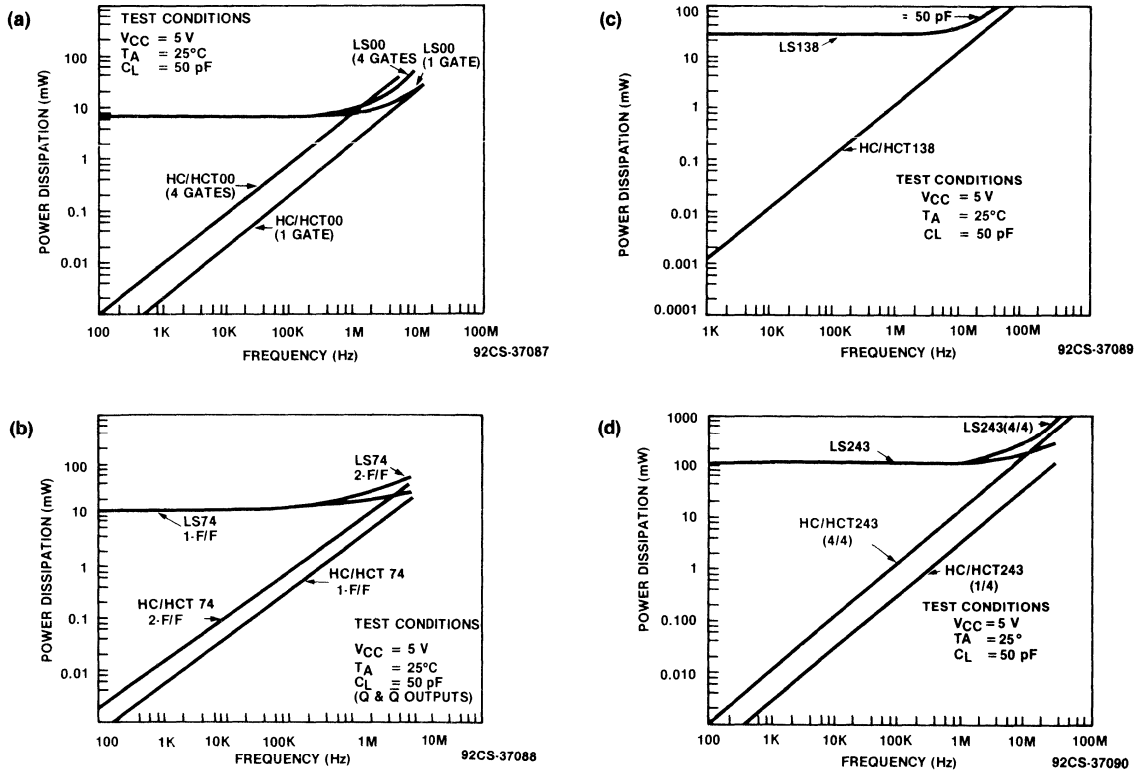
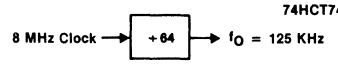



**Fig. 14—Power versus frequency graphs for the (a) LS/HC00, (b) LS/HC74, (c) LS/HCT138, and (d) LS/HC243.**

In most systems, the percentage of the total system operating at the maximum frequency is small because most of the system is clocked at frequencies much lower than the master clock frequency. Thus, even a small system composed of QMOS devices, whose power dissipation is proportional to switching frequency, will exhibit substantial savings in power consumption in relation to a comparable LSTTL system. Table VI shows an excellent example of the power savings obtainable.

**Table VI—Example of Power Savings**

74HCT74 CMOS vs 74LS74 TTL




**USE 6 "D" FF OR 3 74XX74 IC's**

| STAGE | IC-1 | | IC-2 | | IC-3 | | |
|---|---|---|---|---|---|---|---|
| | #1 ÷2 | #2 ÷2 | #3 ÷2 | #4 ÷2 | #5 ÷2 | #6 ÷2 | — |
| $f_{IN}$ (MHz) | 8 | 4 | 2 | 1 | 0.5 | 0.25 | — |
| 74LS74 POWER (mW) | 22.0 | 18.0 | 16.0 | 14.0 | 13.0 | 12.0 | LS TOTAL 95 mW |
| 74HCT74 POWER (mW) | 15.0 | 8.0 | 4.0 | 2.0 | 1.0 | 0.5 | HCT TOTAL 30.5 |
| % POWER SAVING CMOS/LSTTL | 32 | 55 | 75 | 86 | 92 | 96 | NET % POWER SAVING 68 |

*Power-Supply Requirements* — The average power consumption of QMOS systems is usually low, and can be predicted by summing the total power for each QMOS logic function using equation 5. The bulk of this power dissipation is caused by transient switching currents; therefore, the power supply used should be able to supply this transient current. In addition, a decoupling capacitor of 10 nF per standard output device is suggested. For octal bus-driver devices, a 0.1 $\mu$F capacitance connected from $V_{CC}$ to ground is suggested as a means of absorbing the switching-transient current.

### Interfacing and Noise Margins

Because of the characteristics of the CMOS output, the QMOS family is very versatile in interfacing between different logic families. This capability including the corresponding fanout is illustrated in Figure 15.

Note that the fanout to CMOS devices is limited only by the input rise and fall times, which are dependent on the capacitive loading, $C_L$. This dependence can be computed by the following relationship:

$$t_r, t_f = 2.2\ RC_L \qquad (6)$$

where R is the impedance of the output.

The QMOS HC types cannot be driven from any of the TTL families because the TTL output voltage high, $V_{OH}$(min), does not satisfy the HC input voltage high, $V_{IH}$(min), specification. The HCT types can be directly interfaced to the TTL families because the HCT input voltage high, $V_{IH}$(min), specification is less than the TTL output voltage high, $V_{OH}$(min). The problem with the HC types can be eliminated by using a pull-up resistor as illustrated in Figure 16,

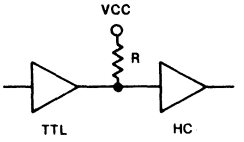



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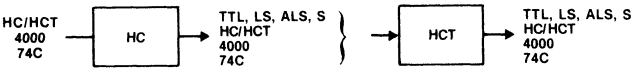
**Fig. 16—Use of pull-up resistor to interface TTL and HC devices.**

however this method will cause degradation of the following QMOS characteristics:

1. dynamic performance — increases $t_{PHL}$ and $t_{THL}$
2. power consumption — increases when output is logic 0 because of the current path from $V_{CC}$ to ground through the resistor
3. fanout — decreases because of current requirement through resistor
4. noise margin — decreases because of increase in $V_{OL}$ (max)
5. reliability — increases component count and the number of solder joints

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| Fanout From: | *To Corresponding Logic Families:* | | | | | |
|---|---|---|---|---|---|---|
| HC/HCT | TTL | LS | ALS | FAST | S/AS | 4000, 74C |
| Standard Types | 2 | 10 | 20 | 6 | 2 | See Text |
| Bus Drivers | 3 | 15 | 30 | 10 | 3 | |

**Fig. 15—QMOS interfacing capability and corresponding fanout to other logic families.**

**Table VII—Comparison of Noise Margins Resulting from the Interfacing of HC/HCT-series QMOS devices with other logic products**

$T_A$ = -55°C to +125°C
$V_{CC}$ = 5 V ± 10%

| | | | | | NOISE MARGIN | | IMPROVEMENT MULTIPLIER HC/HCT TO LSTTL | |
|---|---|---|---|---|---|---|---|---|
| | $V_{OL}$ | $V_{OH}$ | $V_{IL}$ | $V_{IH}$ | $V_{NH} = V_{IL}-V_{OL}$ | $V_{NH} = V_{OH}-V_{IH}$ | NOISE MARGIN LOW | NOISE MARGIN HIGH |
| HC TO HC | 0.1 V | 4.9 V | 1.0 V | 3.5 V | 0.9 V | 1.4 V | 2.25 | 2.0 |
| HC TO HCT | 0.1 V | 4.9 V | 0.8 V | 2.0 V | 0.7 V | 2.9 V | 1.75 | 4.14 |
| HC, HCT TO LS | 0.4 V | 3.7 V | 0.8 V | 2.0 V | 0.4 V | 1.7 V | 1.0 | 2.43 |
| LS TO LS | 0.4 V | 2.7 V | 0.8 V | 2.0 V | 0.4 V | 0.7 V | — | — |

When interfacing between logic families, the noise margins will be affected. For optimum noise margins the HC family should be used. The noise margins, normalized to LSTTL, resulting from the interfacing of HC/HCT devices to other families are illustrated in Table VII.

### System (Parallel) Clocking

When utilizing the QMOS family in synchronously clocked systems, the following guidelines should be followed. Because of variations in switching points between devices, a slow clock edge could cause a logic error. If data in one of the synchronously clocked circuits changes before the switching point of the next sequential circuit is reached, a logic error will occur. This situation is illustrated in Figure 17.

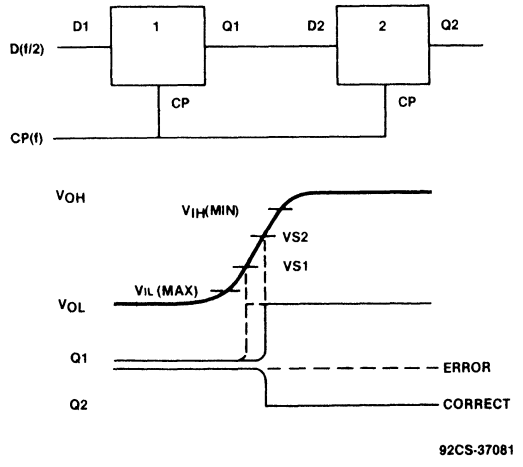



**Fig. 17—Result of changing data in one synchronously clocked circuit before the switching point of the next sequential circuit is reached.**

$V_{S1}$ = Switching point, device 1
$V_{S2}$ = Switching point, device 2
$t_p$ = Propagation delay

Because of variations in input threshold voltages among QMOS HC-version devices, the maximum-clock-pulse rise or fall time should adhere to the following relationship:

$$t_r, t_f \text{ (max)} < 2\ t_p \text{ (max)} \quad (7)$$

In a system where HC, HCT, and TTL-type families are mixed, the maximum clock pulse rise or fall times should adhere to the following relationship:

$$t_r, t_f \text{ (max)} < t_p \text{ (max)} \quad (8)$$

It is recommended that a Schmitt trigger circuit be utilized if wave shaping is required.

The maximum rise or fall time into any QMOS device, HC or HCT, must be limited to 1000, 500, and 400 ns at 2, 4.5, and 6 volts, respectively. If these limits are exceeded, noise on the input or power supply may cause the outputs to oscillate during transition. This oscillation could cause logic errors and unnecessary power consumption.

### Three-State Output and Bus Considerations

In the high-impedance state, the output leakage current is typically less than 2 nA. The current is junction leakage of the turned off NMOS and PMOS output transistors. The maximum output leakage current specifications are ± 0.5, ± 5, and ± 10 μA at 25, 85, and 125°C, respectively.

In applications where operating frequency is greater than or equal to 4 MHz, the bus termination shown in Figure 18 is recommended.

When devices with I/O pins are three-stated, it is important to have the inputs terminated, as explained in the section on **Input Characteristics.** In systems where buses or PC cards may be removed while power is on, it is recommended that inputs connected to the peripheral be terminated to $V_{CC}$ or ground through a 10k resistor, as shown in Figure 19.

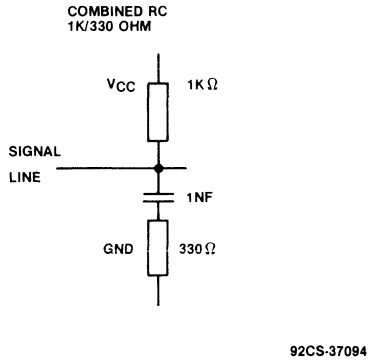



**Fig. 18—Recommended Bus Terminations (Information courtesy of Beradine Products, BC, Canada.)**

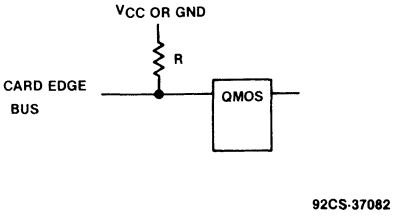



**Fig. 19—Method of handling inputs in systems where buses or PC cords may be removed while power is on.**

# Standardized Capacitance Power Dissipation (CPD) Test Procedure

The purpose of the CPD number is to allow the user to estimate the actual power consumption of his system. Therefore, the table has been set up to exercise each device in the same manner as it would usually be used. Devices which are separable into independent sections are measured on a "per section" basis, the remaining are measured on a "per device" basis. Each part number's unique setup is listed in the "Pin Condition Table." The following paragraphs describe the generic set up for each class of devices:

**All part numbers:** Measurements are to be made at $T_A$ = 25°C, $V_{CC}$ = 5V, and 3-state outputs both enabled and disabled.

**Gates:** Switch one input. Bias the remaining inputs such that the output switches.

**Latches:** Toggle as in a flip-flop.

**Flip-flops:** Switch the clock pin while changing "D" (or biasing "J" and "K") such that the output(s) change each clock cycle. For part numbers with common clocks, exercise the "D", "J", or "K" inputs of only one flip-flop. Set the inputs of the remaining flip-flops so they do not change state.

**Decoders / Demultiplexers:** Switch one address pin, which changes two outputs.

**Data Selectors / Multiplexers:** Switch one address input, with the corresponding data inputs at opposite logic levels, so that the output switches.

**Counters:** Switch the clock pin, with other inputs biased, such that the device counts.

**Shift Registers:** Switch the clock, adjust the data inputs such that the shift register fills with alternate 1's and 0's.

**Transceivers:** Switch one data input. For bi-directional transceivers enable only one direction.

**One Shots:** TO BE DETERMINED

**Parity Generators:** Switch one input.

**Priority Encoders:** Switch the lowest priority input.

**Rams:** TO BE DETERMINED

**Display Drivers:** Switch one input such that approximately half the outputs change state.

**ALUs / Adders:** Switch one least significant input bit, bias the remaining inputs so that the the device is alternately adding 0000 (binary) or 0001 (binary) to 1111 (binary).

Since CPD is a measure of device power consumption, and not that of the driven load, each output would ideally be unloaded. However, this is impractical with automatic testers which often have 30 to 40 pF hanging on each pin. Therefore, each output which is switching should be loaded with the standard 50 pF. The equivalent load capacitance, based on the number of outputs switching and their frequency, is then subtracted from the measured gross CPD number to obtain the device's actual CPD value.

If a device is tested at a high enough frequency, static supply current will contribute a negligible amount to power consumption and can be ignored. Thus, it is recommended that power consumption be measured at 1 MHz and the following formula be used to calculate CPD:

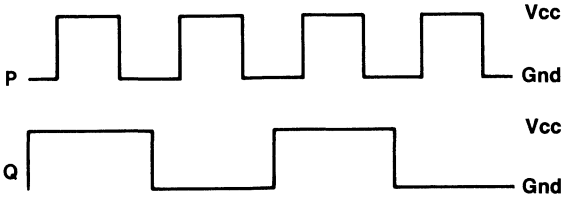
$$CPD = \frac{(I_{CC})}{(V_{CC})(1E6)} - \text{(equivalent load capacitance)}$$

## EXPLANATION OF SYMBOLS

The following symbols are used in the CPD tables:

- V = Vcc (+5 volts)
- G = Ground
- H = Logic 1 (Vcc) — Inputs at Vcc for HC types, 3.5V for HCT types
- L = Logic 0 (ground)
- D = Don't care — either H or L but not switching
- C = A 50 pF load to ground
- O = An open pin; 50 pF to ground is OK
- P = Input pulse (see illustration)
- Q = Half frequency pulse (see illustration)

**Input Pulses**

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**Pin Condition Table**

| CD54/74 HC/HCT | Equiv. load (pF) | Pin Number | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
| 00 | 50 | P | H | C | D | D | O | G | O | D | D | O | D | D | V | • | • | • | • | • | • | • | • | • | • |
| 02 | 50 | C | P | L | O | D | D | G | D | D | O | D | D | O | V | • | • | • | • | • | • | • | • | • | • |
| 04 | 50 | P | C | D | O | D | O | G | O | D | O | D | O | D | V | • | • | • | • | • | • | • | • | • | • |
| 08 | 50 | P | H | C | D | D | O | G | O | D | D | O | D | D | V | • | • | • | • | • | • | • | • | • | • |
| 10 | 50 | P | H | D | D | D | O | G | O | D | D | D | C | H | V | • | • | • | • | • | • | • | • | • | • |
| 11 | 50 | P | H | D | D | D | O | G | O | D | D | D | C | H | V | • | • | • | • | • | • | • | • | • | • |
| 14 | 50 | P | C | D | O | D | O | G | O | D | O | D | O | D | V | • | • | • | • | • | • | • | • | • | • |
| 20 | 50 | P | H | O | H | H | C | G | O | D | D | O | D | D | V | • | • | • | • | • | • | • | • | • | • |
| 27 | 50 | P | L | D | D | D | O | G | O | D | D | D | C | L | V | • | • | • | • | • | • | • | • | • | • |
| 32 | 50 | P | L | C | D | D | O | G | O | D | D | O | D | D | V | • | • | • | • | • | • | • | • | • | • |
| 42 | 100 | C | C | O | O | O | O | O | G | O | O | O | L | L | L | P | V | • | • | • | • | • | • | • | • |
| 73 | 50 | P | H | H | V | D | D | D | O | O | D | G | C | C | H | • | • | • | • | • | • | • | • | • | • |
| 74 | 50 | H | Q | P | H | C | C | G | O | O | D | D | D | D | V | • | • | • | • | • | • | • | • | • | • |
| 75 | 100 | C | P | D | D | V | D | D | O | O | O | O | G | H | O | O | C | • | • | • | • | • | • | • | • |
| 85 | 50 | L | H | P | H | O | C | O | G | L | L | L | L | L | L | L | V | • | • | • | • | • | • | • | • |
| 86 | 50 | P | L | C | D | D | O | G | O | D | D | O | D | D | V | • | • | • | • | • | • | • | • | • | • |
| 107 | 50 | H | C | C | H | O | O | G | D | D | H | D | P | H | V | • | • | • | • | • | • | • | • | • | • |
| 109 | 50 | H | H | L | P | H | C | C | G | O | O | H | D | D | D | H | V | • | • | • | • | • | • | • | • |
| 112 | 50 | P | H | H | H | C | C | O | G | O | H | D | D | D | H | H | V | • | • | • | • | • | • | • | • |
| 123* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 132 | 50 | P | H | C | D | D | O | G | O | D | D | O | D | D | V | • | • | • | • | • | • | • | • | • | • |
| 138 | 100 | P | L | L | L | L | H | O | G | O | O | O | O | O | C | C | V | • | • | • | • | • | • | • | • |
| 139 | 100 | L | P | L | C | C | O | O | G | O | O | O | O | D | D | D | V | • | • | • | • | • | • | • | • |
| 147 | 100 | H | H | H | H | H | O | O | G | C | H | P | H | H | O | O | V | • | • | • | • | • | • | • | • |
| 151 | 100 | D | D | L | H | C | C | L | G | L | L | P | D | D | D | D | V | • | • | • | • | • | • | • | • |
| 153 | 50 | L | L | D | D | L | H | C | G | O | L | L | D | D | P | D | V | • | • | • | • | • | • | • | • |
| 154 | 100 | C | C | O | O | O | O | O | O | O | O | O | G | O | O | O | O | O | L | L | L | L | L | P | V |
| 157 | 50 | P | L | H | C | L | L | O | G | O | L | L | O | L | L | L | V | • | • | • | • | • | • | • | • |
| 158 | 50 | P | L | H | C | L | L | O | G | O | L | L | O | L | L | L | V | • | • | • | • | • | • | • | • |
| 160 | 50 | H | P | D | D | D | D | H | G | H | H | C | C | C | C | C | V | • | • | • | • | • | • | • | • |
| 161 | 50 | H | P | D | D | D | D | H | G | H | H | C | C | C | C | C | V | • | • | • | • | • | • | • | • |
| 162 | 50 | H | P | D | D | D | D | H | G | H | H | C | C | C | C | C | V | • | • | • | • | • | • | • | • |
| 163 | 50 | H | P | D | D | D | D | H | G | H | H | C | C | C | C | C | V | • | • | • | • | • | • | • | • |
| 164 | 200 | Q | Q | C | C | C | C | G | P | H | C | C | C | C | V | • | • | • | • | • | • | • | • | • | • |
| 165 | 50 | H | P | D | D | D | D | C | G | C | Q | D | D | D | D | L | V | • | • | • | • | • | • | • | • |
| 166 | 25 | Q | D | D | D | D | L | P | G | H | D | D | D | C | D | H | V | • | • | • | • | • | • | • | • |
| 173 | 25 | L | L | C | O | O | O | P | G | L | L | D | D | D | Q | L | V | • | • | • | • | • | • | • | • |
| 174 | 25 | H | C | Q | D | O | D | O | G | P | O | D | O | D | D | O | V | • | • | • | • | • | • | • | • |

* Conditions to be established at a later date

## Pin Condition Table (Cont'd)

| CD54/74 HC/HCT | Equiv. load (pF) | Pin Number | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
| 175 | 50 | H | C | C | Q | D | O | O | G | P | O | O | D | D | O | O | V | • | • | • | • | • | • | • | • |
| 190 | 53 | D | C | C | L | L | C | C | G | D | D | H | C | C | P | D | V | • | • | • | • | • | • | • | • |
| 191 | 53 | D | C | C | L | L | C | C | G | D | D | H | C | C | P | D | V | • | • | • | • | • | • | • | • |
| 192 | 50 | D | C | C | H | P | C | C | G | D | D | H | C | C | L | D | V | • | • | • | • | • | • | • | • |
| 193 | 50 | D | C | C | H | P | C | C | G | D | D | H | C | C | L | D | V | • | • | • | • | • | • | • | • |
| 194 | 100 | H | Q | D | D | D | D | D | G | H | L | P | C | C | C | C | V | • | • | • | • | • | • | • | • |
| 195 | 125 | H | H | L | D | D | D | D | G | H | P | C | C | C | C | C | V | • | • | • | • | • | • | • | • |
| 221* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 238 | 100 | P | L | L | L | L | H | O | G | O | O | O | O | O | C | C | V | • | • | • | • | • | • | • | • |
| 240 | 50 | L | P | O | D | O | D | O | D | O | G | D | O | D | O | D | O | D | C | L | V | • | • | • | • |
| 241 | 50 | L | P | O | D | O | D | O | D | O | G | D | O | D | O | D | O | D | C | H | V | • | • | • | • |
| 242 | 50 | L | O | P | D | D | D | G | O | O | O | C | O | L | V | • | • | • | • | • | • | • | • | • | • |
| 243 | 50 | L | O | P | D | D | D | G | O | O | O | C | O | L | V | • | • | • | • | • | • | • | • | • | • |
| 244 | 50 | L | P | O | D | O | D | O | D | O | G | D | O | D | O | D | O | D | C | L | V | • | • | • | • |
| 245 | 50 | H | P | D | D | D | D | D | D | D | G | O | O | O | O | O | O | O | C | L | V | • | • | • | • |
| 251 | 100 | D | D | L | H | C | C | L | G | L | L | P | D | D | D | D | V | • | • | • | • | • | • | • | • |
| 253 | 50 | L | L | D | D | L | H | C | G | O | L | L | D | D | P | L | V | • | • | • | • | • | • | • | • |
| 257 | 50 | P | L | H | C | L | L | O | G | O | L | L | O | L | L | L | V | • | • | • | • | • | • | • | |
| 259 | 25 | L | L | L | C | O | O | O | G | O | O | O | O | Q | P | H | V | • | • | • | • | • | • | • | • |
| 273 | 25 | H | C | Q | D | O | O | D | D | O | G | P | O | D | D | O | O | D | D | O | V | • | • | • | • |
| 280 | 100 | P | L | O | L | C | C | G | L | L | L | L | L | L | V | • | • | • | • | • | • | • | • | • | • |
| 297* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 299 | 250 | H | L | L | C | C | C | C | C | H | G | Q | P | C | C | C | C | C | D | L | V | • | • | • | • |
| 354 | 100 | D | D | D | D | D | D | L | H | L | G | L | L | L | P | L | L | H | C | C | V | • | • | • | • |
| 356 | 50 | D | D | D | D | D | D | D | Q | P | G | L | L | L | L | L | L | H | C | C | V | • | • | • | • |
| 365 | 50 | L | P | C | D | O | D | O | G | O | D | O | D | O | D | L | V | • | • | • | • | • | • | • | • |
| 366 | 50 | L | P | C | D | O | D | O | G | O | D | O | D | O | D | L | V | • | • | • | • | • | • | • | • |
| 367 | 50 | L | P | C | D | O | D | O | G | O | D | O | D | O | D | L | V | • | • | • | • | • | • | • | • |
| 368 | 50 | L | P | C | D | O | D | O | G | O | D | O | D | O | D | L | V | • | • | • | • | • | • | • | • |
| 373 | 50 | L | C | P | D | O | O | D | D | O | G | H | O | D | D | O | O | D | D | O | V | • | • | • | • |
| 374 | 25 | L | C | Q | D | O | O | D | D | O | G | P | O | D | D | O | O | D | D | O | V | • | • | • | • |
| 377 | 25 | L | C | Q | D | O | O | D | D | O | G | P | O | D | D | O | O | D | D | O | V | • | • | • | • |
| 384* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 390 | 45 | P | L | C | Q | C | C | C | G | O | O | O | D | O | L | D | V | • | • | • | • | • | • | • | • |
| 393 | 47 | P | L | C | C | C | C | G | O | O | O | O | D | L | V | • | • | • | • | • | • | • | • | • | • |
| 423* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 533 | 50 | L | C | P | D | O | O | D | D | O | G | H | O | D | D | O | O | D | D | O | V | • | • | • | • |
| 534 | 25 | L | C | Q | D | O | O | D | D | O | G | P | O | D | D | O | O | D | D | O | V | • | • | • | • |
| 540 | 50 | L | P | D | D | D | D | D | D | D | G | O | O | O | O | O | O | O | C | L | V | • | • | • | • |
| 541 | 50 | L | P | D | D | D | D | D | D | D | G | O | O | O | O | O | O | O | C | L | V | • | • | • | • |
| 563 | 50 | L | P | D | D | D | D | D | D | D | G | H | O | O | O | O | O | O | C | V | • | • | • | • | • |
| 564 | 25 | L | Q | D | D | D | D | D | D | D | G | P | O | O | O | O | O | O | C | V | • | • | • | • | • |
| 573 | 50 | L | P | D | D | D | D | D | D | D | G | H | O | O | O | O | O | O | C | V | • | • | • | • | • |
| 574 | 25 | L | Q | D | D | D | D | D | D | D | G | P | O | O | O | O | O | O | C | V | • | • | • | • | • |
| 640 | 50 | H | P | D | D | D | D | D | D | D | G | O | O | O | O | O | O | C | L | V | • | • | • | • | • |
| 643 | 50 | H | P | D | D | D | D | D | D | D | G | O | O | O | O | O | O | C | L | V | • | • | • | • | • |
| 646 | 50 | D | L | H | P | D | D | D | D | D | D | D | G | O | O | O | O | O | O | C | L | D | D | V | |
| 648 | 50 | D | L | H | P | D | D | D | D | D | D | D | G | O | O | O | O | O | O | C | L | D | D | V | |
| 670 | 50 | D | D | D | L | L | O | O | G | O | C | L | L | L | L | P | V | • | • | • | • | • | • | • | • |
| 688 | 50 | L | P | L | H | H | L | L | H | H | G | L | L | H | H | L | L | H | H | C | V | • | • | • | • |
| 4002 | 50 | C | P | L | L | L | O | G | O | D | D | D | O | V | • | • | • | • | • | • | • | • | • | • | • |
| 4015 | 100 | P | C | O | O | O | D | D | G | D | O | C | C | C | L | Q | V | • | • | • | • | • | • | • | • |
| 4016* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 4017 | 55 | C | C | C | C | C | C | C | G | C | C | C | C | L | P | L | V | • | • | • | • | • | • | • | • |
| 4020 | 31 | C | C | C | C | C | C | C | G | C | P | L | C | C | C | C | V | • | • | • | • | • | • | • | • |
| 4024 | 50 | P | L | C | C | C | C | G | O | C | O | C | C | O | V | • | • | • | • | • | • | • | • | • | • |
| 4040 | 50 | C | C | C | C | C | C | C | G | C | P | L | C | C | C | C | V | • | • | • | • | • | • | • | • |
| 4046* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 4049 | 50 | V | C | P | O | D | O | D | G | D | O | D | O | O | D | O | O | • | • | • | • | • | • | • | • |

* Conditions to be established at a later date

**Pin Condition Table (Cont'd)**

| CD54/74 HC/HCT | Equiv. load (pF) | Pin Number | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
| 4050 | 50 | V | C | P | O | D | O | D | G | D | O | D | O | O | D | O | O | • | • | • | • | • | • | • | • |
| 4051* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 4052* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 4053* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 4060 | 150 | C | C | C | C | C | C | C | G | C | C | P | L | C | C | C | V | • | • | • | • | • | • | • | • |
| 4066* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 4067* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 4075 | 50 | P | L | D | D | D | O | G | L | C | O | D | D | D | V | • | • | • | • | • | • | • | • | • | • |
| 4094* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 4511 | 200 | L | L | H | H | L | L | P | G | C | C | O | O | C | O | C | V | • | • | • | • | • | • | • | • |
| 4514 | 100 | H | P | L | O | O | O | O | O | C | O | C | G | O | O | O | O | O | O | O | O | L | L | L | V |
| 4515 | 100 | H | P | L | O | O | O | O | O | C | O | C | G | O | O | O | O | O | O | O | O | L | L | L | V |
| 4518 | 45 | P | H | C | C | C | C | L | G | D | D | O | O | O | O | D | V | • | • | • | • | • | • | • | • |
| 4520 | 47 | P | H | C | C | C | C | L | G | D | D | O | O | O | O | D | V | • | • | • | • | • | • | • | • |
| 4538* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 4543* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 40102* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 40103* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 40104* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| 40105* | — | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |

* Conditions to be established at a later date

# RCA Standardized Maximum Ratings and Recommended Operating Conditions for CD54/74HC, CD54/74HCT, and CD54/74HCU QMOS Integrated Circuits

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5$ V):
STANDARD OUTPUT ..... ±25 mA
BUS DRIVER OUTPUT ..... ±35 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$):
STANDARD OUTPUT ..... ±50 mA
BUS DRIVER OUTPUT ..... ±70 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = -55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

**RECOMMENDED OPERATING CONDITIONS:**
**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$=Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{in}$, $V_{out}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times $t_r$, $t_f$ | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

## Static Electrical Characteristics for CD74HC/CD54HC Types ▲

| | Symb | Parameter | $V_{CC}$ | Temperature °C | | | | | | Unit | Test Conditions | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 54HC/74HC 25 | | 74HC −40 to 85 | | 54HC −55 to 125 | | | | | | |
| | | | V | min | max | min | max | min | max | | | | | |
| | $V_{IH}$ | High Level Input Voltage | 2.0 | 1.5 | | 1.5 | | 1.5 | | V | | | | |
| | | | 4.5 | 3.15 | | 3.15 | | 3.15 | | V | | | | |
| | | | 6.0 | 4.2 | | 4.2 | | 4.2 | | V | | | | |
| | $V_{IL}$ | Low Level Input Voltage | 2.0 | | 0.3 | | 0.3 | | 0.3 | V | | | | |
| | | | 4.5 | | 0.9 | | 0.9 | | 0.9 | V | | | | |
| | | | 6.0 | | 1.2 | | 1.2 | | 1.2 | V | | | | |
| | | | | | | | | | | | $V_I$ | $I_O$ | | |
| | | | | | | | | | | | | STD | BUS | Unit |
| * | $V_{OH}$ | High Level Output Voltage | 2.0 | 1.9 | | 1.9 | | 1.9 | | V | | −20.0 | −20.0 | μA |
| | | | 4.5 | 4.4 | | 4.4 | | 4.4 | | V | | −20.0 | −20.0 | μA |
| | | | 6.0 | 5.9 | | 5.9 | | 5.9 | | V | $V_{IH}$ or $V_{IL}$ | −20.0 | −20.0 | μA |
| | | | 4.5 | 3.86 | | 3.76 | | 3.7 | | V | | −4.0 | −6.0 | mA |
| | | | 6.0 | 5.36 | | 5.26 | | 5.2 | | V | | −5.2 | −7.8 | mA |
| * | $V_{OL}$ | Low Level Output Voltage | 2.0 | | 0.1 | | 0.1 | | 0.1 | V | | 20.0 | 20.0 | μA |
| | | | 4.5 | | 0.1 | | 0.1 | | 0.1 | V | | 20.0 | 20.0 | μA |
| | | | 6.0 | | 0.1 | | 0.1 | | 0.1 | V | $V_{IH}$ or $V_{IL}$ | 20.0 | 20.0 | μA |
| | | | 4.5 | | 0.32 | | 0.37 | | 0.4 | V | | 4.0 | 6.0 | mA |
| | | | 6.0 | | 0.32 | | 0.37 | | 0.4 | V | | 5.2 | 7.8 | mA |
| | $I_I$ + | Input Leakage Current | 6.0 | | ±0.1 | | ±1.0 | | ±1.0 | μA | $V_I = V_{CC}$ or GND | | | |
| | $I_{S(off)}$ | Analog Switch Off-State Current Per Channel | 6.0 | | ±0.1 | | ±1.0 | | ±1.0 | μA | $V_I = V_{IH}$ or $V_{IL}$<br>$\|V_S\| = V_{CC}$ or $V_{CC} - V_{EE}$ | | | |
| | $I_{OZ}$ | 3-state Output Off-State Current | 6.0 | | ±0.5 | | ±5.0 | | ±10.0 | μA | $V_I = V_{IH}$ or $V_{IL}$<br>$V_O = V_{CC}$ or GND | | | |
| | $I_{CC}$ | Quiescent Supply Current | | | | | | | | | $V_I = V_{CC}$ or GND | | | |
| | | SSI | 6.0 | | 2.0 | | 20.0 | | 40.0 | μA | | | | |
| | | FF | 6.0 | | 4.0 | | 40.0 | | 80.0 | μA | $I_O = 0$ | | | |
| | | MSI | 6.0 | | 8.0 | | 80.0 | | 160. | μA | | | | |

▲ Reprinted from JEDEC Tentative Standard No. 7, "Standard Specification for Description of 54/74HCXXX, 54/74HCUXXX, and 54/74HCTXXX High Speed CMOS Devices".

* Tighter limits imposed on RCA QMOS types. Refer to detailed Preliminary Specifications.

+ For Transceivers use $I_{OZ}$

## Static Electrical Characteristics for CD74HCT/CD54HCT Types ▲

| Symb | Parameter | $V_{CC}$ | Temperature °C | | | | | | Unit | Test Conditions | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 54HCT/74HCT 25 | | 74HCT −40 to 85 | | 54HCT −55 to 125 | | | | | | |
| | | v | min | max | min | max | min | max | | | | | |
| $V_{IH}$ | High Level Input Voltage | 4.5 to 5.5 | 2.0 | | 2.0 | | 2.0 | | v | | | | |
| $V_{IL}$ | Low Level Input Voltage | 4.5 to 5.5 | | 0.8 | | 0.8 | | 0.8 | v | | | | |
| • * $V_{OH}$ | High Level Output Voltage | 4.5 | 4.4 | | 4.4 | | 4.4 | | v | $V_I$: $V_{IH}$ or $V_{IL}$ | $I_O$ STD: −20.0 | $I_O$ BUS DRIVER: −20.0 | Unit: μA |
| | | 4.5 | 3.86 | | 3.76 | | 3.7 | | v | | −4.0 | −6.0 | mA |
| * $V_{OL}$ | Low Level Output Voltage | 4.5 | | 0.1 | | 0.1 | | 0.1 | v | $V_{IH}$ or $V_{IL}$ | −20.0 | −20.0 | μA |
| | | 4.5 | | 0.32 | | 0.37 | | 0.4 | v | | −4.0 | −6.0 | mA |
| $I_I$ + | Input Leakage Current | 5.5 | | ±0.1 | | ±1.0 | | ±1.0 | μA | $V_I = V_{CC}$ or GND | | | |
| $I_I$ | Input Leakage Current | 5.5 | | | | | | | mA | $V_I = V_{IH}$ or $V_{IL}$ | | | |
| $I_{S(off)}$ | Analog Switch Off-State Current Per Channel | 5.5 | | ±0.1 | | ±1.0 | | ±1.0 | μA | $V_I = V_{IH}$ or $V_{IL}$; $\|V_S\| = V_{CC}$ or $V_{CC} - V_{EE}$ | | | |
| $I_{OZ}$ | 3-state Output Off-State Current | 5.5 | | ±0.5 | | ±5.0 | | ±10.0 | μA | $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND | | | |
| $I_{CC}$ | Quiescent Supply Current | | | | | | | | | | | | |
| | SSI | 5.5 | | 2.0 | | 20.0 | | 40.0 | μA | $V_I = V_{CC}$ or GND | | | |
| | FF | 5.5 | | 4.0 | | 40.0 | | 80.0 | μA | $I_O = 0$ | | | |
| | MSI | 5.5 | | 8.0 | | 80.0 | | 160. | μA | | | | |
| $I_C$ | Maximum Quiescent Supply Current | 5.5 | | | | | | | mA | Per input-pin: $V_{IN} = 2.4V$ or $V_{IN} = 0.5V$ | Other inputs: at $V_{CC}$ or GND; $I_O = 0$ | | |

▲ Reprinted from JEDEC Tentative Standard No. 7, "Standard Specification for Description of 54/74HCXXX, 54/74HCUXXX, and 54/74HCTXXX High Speed CMOS Devices".

* Tighter limits imposed on RCA QMOS types. Refer to detailed Preliminary Specifications.

+ For Transceivers use $I_{OZ}$

# Static Electrical Characteristics for CD74HCU/CD54HCU Types ▲

| Symb | Parameter | $V_{CC}$ | Temperature °C | | | | | | Unit | Test Conditions | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 54HCU/74HCU 25 | | 74HCU −40 to 85 | | 54HCU −55 to 125 | | | | | | | |
| | | v | min | max | min | max | min | max | | | | | | |
| $V_{IH}$ | High Level Input Voltage | 2.0 | 1.7 | | 1.7 | | 1.7 | | v | | | | | |
| | | 4.5 | 3.6 | | 3.6 | | 3.6 | | v | | | | | |
| | | 6.0 | 4.8 | | 4.8 | | 4.8 | | v | | | | | |
| $V_{IL}$ | Low Level Input Voltage | 2.0 | | 0.3 | | 0.3 | | 0.3 | v | | | | | |
| | | 4.5 | | 0.8 | | 0.8 | | 0.8 | v | | | | | |
| | | 6.0 | | 1.1 | | 1.1 | | 1.1 | v | | | | | |
| | | | | | | | | | | $V_I$ | $I_O$ | | | |
| | | | | | | | | | | | — | — | Unit | |
| * $V_{OH}$ | High Level Output Voltage | 2.0 | 1.8 | | 1.8 | | 1.8 | | v | $V_{IH}$ or $V_{IL}$ | | − 20.0 | μA | |
| | | 4.5 | 4.0 | | 4.0 | | 4.0 | | v | | | − 20.0 | μA | |
| | | 6.0 | 5.5 | | 5.5 | | 5.5 | | v | | | − 20.0 | μA | |
| | | 4.5 | 3.86 | | 3.76 | | 3.7 | | v | $V_{CC}$ or GND | | − 4.0 | mA | |
| | | 6.0 | 5.36 | | 5.26 | | 5.2 | | v | | | − 5.2 | mA | |
| * $V_{OL}$ | Low Level Output Voltage | 2.0 | | 0.2 | | 0.2 | | 0.2 | v | $V_{IH}$ or $V_{IL}$ | | 20.0 | μA | |
| | | 4.5 | | 0.5 | | 0.5 | | 0.5 | v | | | 20.0 | μA | |
| | | 6.0 | | 0.5 | | 0.5 | | 0.5 | v | | | 20.0 | μA | |
| | | 4.5 | | 0.32 | | 0.37 | | 0.4 | v | $V_{CC}$ or GND | | 4.0 | mA | |
| | | 6.0 | | 0.32 | | 0.37 | | 0.4 | v | | | 5.2 | mA | |
| $I_I$ | Input Leakage Current | 6.0 | | ± 0.1 | | ± 1.0 | | ± 1.0 | μA | $V_I = V_{CC}$ or GND | | | | |
| $I_{CC}$ | Quiescent Supply Current | | | | | | | | | $V_I = V_{CC}$ or GND | | | | |
| | SSI | 6.0 | | 2.0 | | 20.0 | | 40.0 | μA | | | | | |
| | FF | 6.0 | | 4.0 | | 40.0 | | 80.0 | μA | $I_O = 0$ | | | | |
| | MSI | 6.0 | | 8.0 | | 80.0 | | 160. | μA | | | | | |

▲ Reprinted from JEDEC Tentative Standard No. 7, "Standard Specification for Description of 54/74HCXXX, 54/74HCUXXX, and 54/74HCTXXX High Speed CMOS Devices".

* Tighter limits imposed on RCA QMOS types. Refer to detailed Preliminary Specifications.

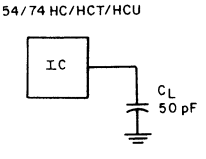
## Dynamic Electrical Characteristics

**Definitions**

| Characteristic | Symbol | Limits | | Notes |
|---|---|---|---|---|
| | | Max. | Min. | |
| Propagation Delay: | | | | |
| Outputs going high to low | $t_{PHL}$ | X | | |
| Outputs going low to high | $t_{PLH}$ | X | | |
| Output Transition Time: | | | | |
| Outputs going high to low | $t_{THL}$ | X | | |
| Outputs going low to high | $t_{TLH}$ | X | | |
| Pulse Width-Set, Reset, Preset Enable, Disable, Strobe, Clock | $t_{WL}$ or $t_{WH}$ | | X | 1 |
| Clock Input Frequency | $f_{CL}$ | X | | 1,2 |
| Clock Input Rise and Fall Time | $t_{rCL}$, $t_{fCL}$ | X | | |
| Set-Up Time | $t_{SU}$ | | X | 1 |
| Hold Time | $t_H$ | | X | 1 |
| Removal Time - Set, Reset, Preset-Enable | $t_{REM}$ | | X | 1 |
| Three State Disable Delay Times: | | | | |
| High level to high impedance | $t_{PHZ}$ | X | | |
| High impedance to low level | $t_{PZL}$ | X | | |
| Low level to high impedance | $t_{PLZ}$ | X | | |
| High impedance to high level | $t_{PZH}$ | X | | |

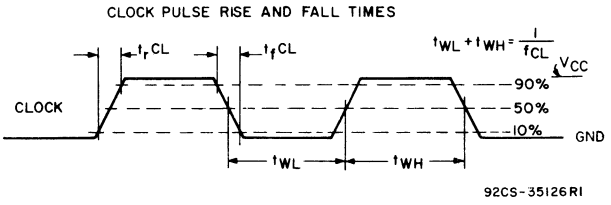
NOTE: (1) By placing a defining min. or max. in front of definition, the limits can change from min. to max., or vice versa.

(2) Clock input waveform should have a 50% duty cycle and be such as to cause the outputs to be switching from 10% $V_{CC}$ to 90% $V_{CC}$ in accordance with the device truth table.



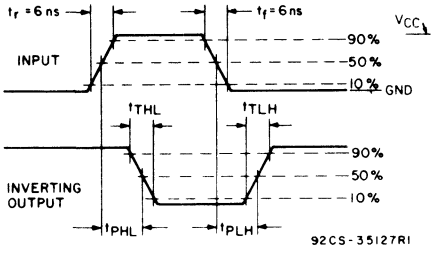

*Test load for associated waveforms shown on pp. 31 and 32.*

# Switching Waveforms for CD54/74HC and CD54/74HCU QMOS Integrated Circuits

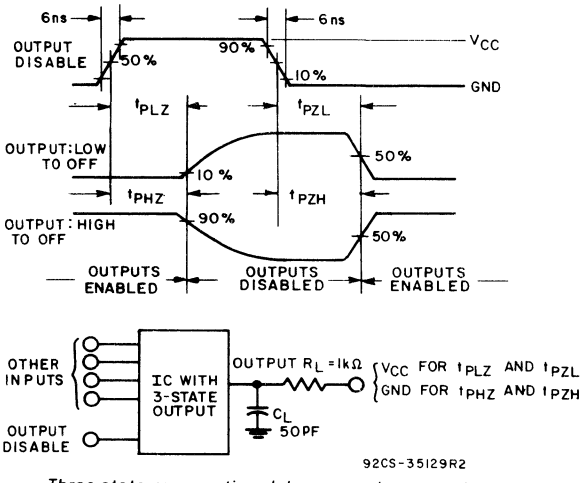



*Outputs should be switching from 10% $V_{CC}$ to 90% $V_{CC}$ in accordance with device truth table. For $f_{max}$, input duty cycle=50%.*

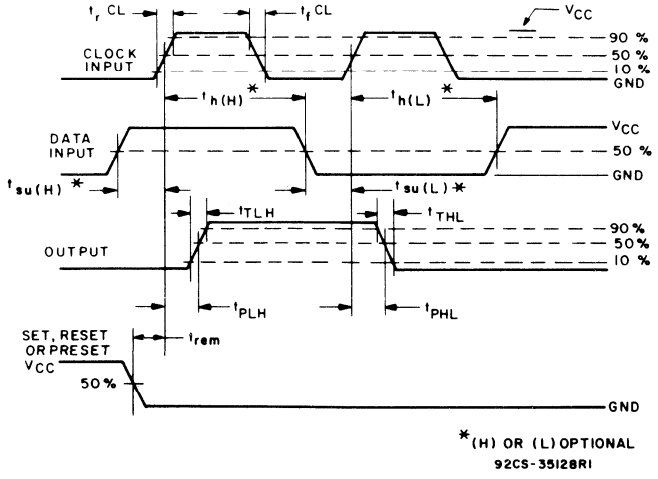
*Clock-pulse rise and fall times and pulse width.*




*Transition times and propagation delay times, combination logic.*

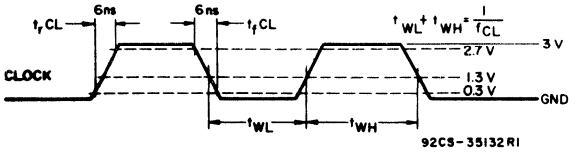



*Three-state propagation delay wave shapes and test circuit.*



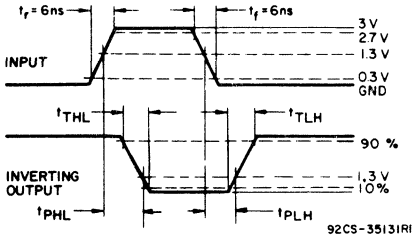

*Setup times, hold times, removal time, and propagation delay times for edge triggered sequential logic circuits.*

# Switching Waveforms for CD54/74HCT QMOS Integrated Circuits

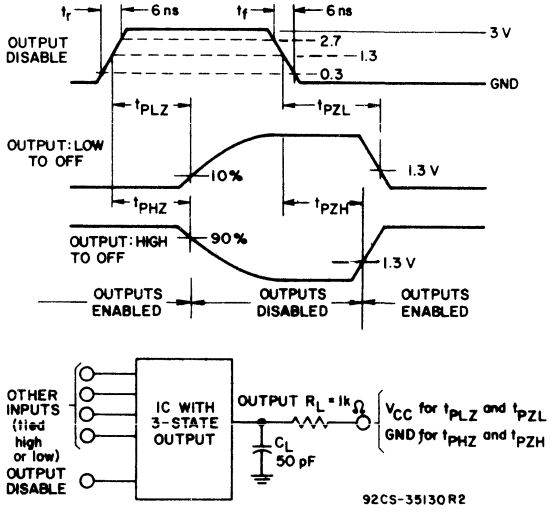



*Outputs should be switching from 10% $V_{CC}$ to 90% $V_{CC}$ in accordance with device truth table. For $f_{max}$, input duty cycle=50%.*

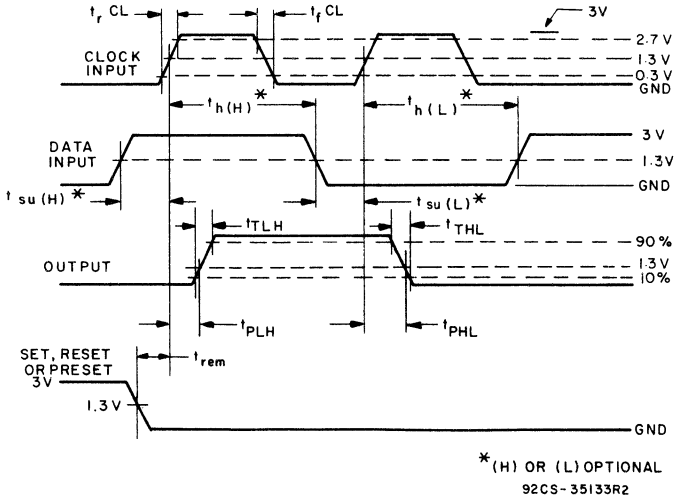
*Clock-pulse rise and fall times and pulse width.*




*Transition times and propagation delay times, combination logic.*




*Three-state propagation delay wave shapes and test circuit.*




*Setup times, hold times, removal time, and propagation delay times for edge triggered sequential logic circuits.*

## Operating and Handling Considerations

1. **Handling**
   All inputs and outputs of RCA CMOS/QMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS/QMOS devices are similar to those described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. **Operating**

**Operating Voltage**

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{CC}$ — Gnd to exceed the absolute maximum rating.

**Input Signals**

To prevent damage to the input protection circuit, input signals should never be greater than $V_{CC}$ nor less than Gnd. Input currents must not exceed 20 mA even when the power supply is off.

**Unused Inputs**

A connection must be provided at every input terminal. All unused input terminals must be connected to either $V_{CC}$ or Gnd, whichever is appropriate.

**Output Short Circuits**

Shorting of outputs to $V_{CC}$ or Gnd may damage CMOS devices by exceeding the maximum device dissipation.

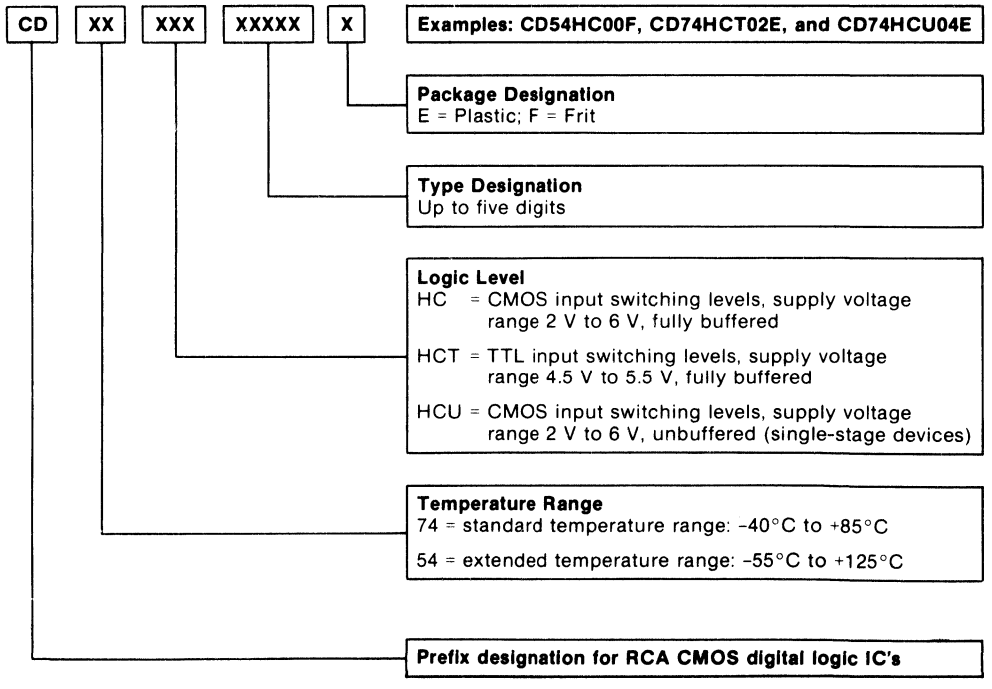
## RCA MIL-STD-883 Slash-Series QMOS IC's

RCA high-reliability slash-series QMOS products will be available in both CD54HCXXXX-series and CD54HCTXXXX-series types. These devices will be supplied in hermetic dual-in-line ceramic packages. The CD54HC/HCT (Slash-series) types will be provided to screening level /3 that corresponds to MIL-STD-883, Method 5004, Class B requirements.

Detailed information pertaining to the screening performed can be found in the RCA "High-Reliability Integrated Circuits" DATABOOK, SSD-230A.

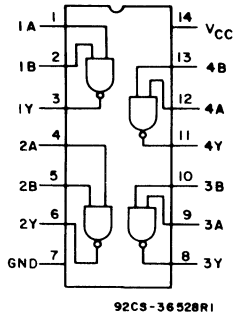
Contact your RCA representative for specific timing and availability.

## QMOS Nomenclature Code




# Technical Data

**Preliminary Data** File Number **1464**




**TERMINAL ASSIGNMENT**

# Quad 2-Input NAND Gate

**Type Features:**

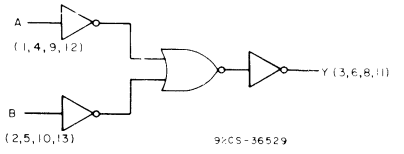
- *Buffered inputs*
- *Typical propagation delay=8 ns @ $V_{CC}$=5 V $C_L$=15 pF, $T_A$=25° C*

**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT/HCU: −40 to +85° C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$=20%, $N_{IH}$=30% of $V_{CC}$ @ $V_{CC}$=5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$=0.8 V Max., $V_{IH}$=2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN} \leq$ 1 μA @ $V_{OL}$, $V_{OH}$*

The RCA-CD54/74HC00 and CD54/74HCT00 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC00 and CD54HCT00 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC00 and CD74HCT00 are supplied in 14-lead dual-in-line plastic packages (E suffix).




**LOGIC DIAGRAM**

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR −0.5 V < $V_o$ < $V_{CC}$ + 0.5 V) ..... ±25 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±50 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = −40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = −55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... −55 to +125° C
PACKAGE TYPE E ..... −40 to +85° C
STORAGE TEMPERATURE ($T_{stg}$) ..... −65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

**RECOMMENDED OPERATING CONDITIONS:**
**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS MIN. | LIMITS MAX. | UNITS |
|---|---|---|---|
| Supply-Voltage Range (For $T_A$=Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{in}$, $V_{out}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times $t_r$,$t_f$ | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC00/CD54HC00 TEST CONDITIONS $V_{IN}$ V | $I_O$ (mA) | $V_{CC}$ V | 74HC/54HC Series +25°C Min | Typ | Max | 74HC Series -40/+85°C Min | Max | 54HC Series -55/+125°C Min | Max | CD74HCT00/CD54HCT00 TEST CONS. $V_{IN}$ V | $V_{CC}$ V | 74HCT/54HCT Series +25°C Min | Typ | Max | 74HCT Series -40/+85°C Min | Max | 54HCT Series -55/+125°C Min | Max | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | — | 4.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | 5.5 | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | — | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | 5.5 | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=-20 μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | — | — | — | — | — | — | — | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) -4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | -5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | — | — | — | — | — | — | — | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20 μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | — | — | — | — | — | — | — | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | — | — | — | — | — | — | — | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) 4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V |
| | | 5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | — | — | — | — | — | — | — | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 2 | — | 20 | — | 40 | $V_{CC}$ or Gnd | 5.5 | — | — | 2 | — | 20 | — | 40 | μA |

**SWITCHING CHARACTERISTICS ($V_{CC}$=5 V, $T_A$=25° C, Input $t_r$,$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | 54/74HC/HCT | |
|---|---|---|---|
| | | Typical | Units |
| Propagation Delay, Data Input to Output Y (Fig. 1) ($C_L$=15 pF) | $t_{PLH}$ $t_{PHL}$ | 8 | ns |
| Input Capacitance | $C_{in}$ | 3.5 | pF |
| Power Dissipation Capacitance* | $C_{PD}$ | 25 | pF |

*$C_{PD}$ is used to determine the dynamic power consumption, per gate.
$PD = C_{PD} Vcc^2 fi + \Sigma C_L Vcc^2 fo$ where fi = input frequency
fo = output frequency
$C_L$ = output load capacitance
Vcc = supply voltage.

**SWITCHING CHARACTERISTICS ($C_L$=50 pF, Input $t_r$=$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay | $t_{PLH}$ | 2 | — | 90 | — | — | — | 115 | — | — | — | 135 | — | — | |
| Input to Output | $t_{PHL}$ | 4.5 | — | 18 | — | 20 | — | 23 | — | 25 | — | 27 | — | 30 | ns |
| (Figure 1) | | 6 | — | 15 | — | — | — | 20 | — | — | — | 23 | — | — | |
| Transition Times | $t_{TLH}$ | 2 | — | 75 | — | — | — | 95 | — | — | — | 110 | — | — | |
| (Figure 1) | $t_{THL}$ | 4.5 | — | 15 | — | 15 | — | 19 | — | 19 | — | 22 | — | 22 | ns |
| | | 6 | — | 13 | — | — | — | 16 | — | — | — | 19 | — | — | |

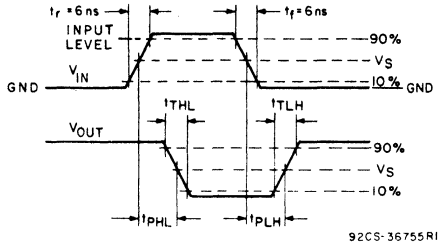
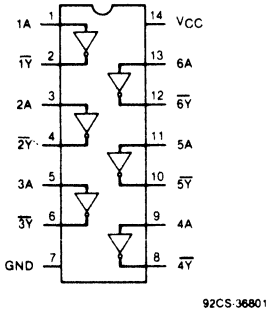



*Fig. 1 - Transition times and propagation delay times, for CD54/74HC.*

File Number **1471**

**Preliminary Data**




**TERMINAL ASSIGNMENT**

# Hex Inverter

**Type Features:**

- *Input and Output are both buffered*
- *Typical propagation delay = 8 ns @ $V_{CC}$ = 5.0 V, $C_L$ = 15 pF, $T_A$ = 25° C*

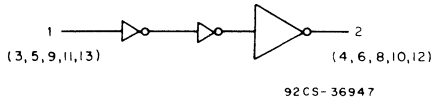
**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT/HCU: -40 to +85° C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*

The RCA-CD54/74HC04 and CD54/74HCT04 hex inverter utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC04 and CD54HCT04 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC04 and CD74HCT04 are supplied in 14-lead dual-in-line plastic packages (E suffix).

- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$ = 20%, $N_{IH}$ = 30% of $V_{CC}$; @ $V_{CC}$ = 5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$ = 0.8 V Max., $V_{IH}$ = 2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN} \leq 1\ \mu A$ @ $V_{OL}$, $V_{OH}$*




**LOGIC DIAGRAM**

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR -0.5 V < $V_O$ < $V_{CC}$ +0.5 V) ..... ±25 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±50 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = -55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

**RECOMMENDED OPERATING CONDITIONS:**
**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply Voltage Range (For $T_A$ = Full Package Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{IN}$, $V_{OUT}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times, $t_r$, $t_f$ | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC04/CD54HC04 | | | | | | | | | | | CD74HCT04/CD54HCT04 | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC Series | | | 74HC Series | | 54HC Series | | | TEST CONS. | | 74HCT/54HCT Series | | | 74HCT Series | | 54HCT Series | | |
| | $V_{IN}$ | | $V_{CC}$ | +25°C | | | -40/ +85°C | | -55/ +125°C | | | $V_{IN}$ | $V_{CC}$ | +25°C | | | -40/ +85°C | | -55/ +125°C | | |
| | V | | V | Min | Typ | Max | Min | Max | Min | Max | | V | V | Min | Typ | Max | Min | Max | Min | Max | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | | — | 4.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | | 5.5 | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | | — | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | | 5.5 | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=-20μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | | — | — | — | — | — | — | — | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) -4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | -5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | | — | — | — | — | — | — | — | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20 μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | — | — | — | — | — | — | — | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) 4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V |
| | | 5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | | — | — | — | — | — | — | — | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 2 | — | 20 | — | 40 | | $V_{CC}$ or Gnd | 5.5 | — | — | 2 | — | 20 | — | 40 | μA |

**SWITCHING CHARACTERISTICS ($V_{CC}$ = 5 V, $T_A$ = 25° C, Input $t_r$ = $t_f$ = 6 ns)**

| CHARACTERISTIC | | 54/74HC/HCT TYPICAL | UNIT |
|---|---|---|---|
| Propagation Delay, Data Input to Output Y (Fig. 1) | $t_{PLH}$ | 8 | ns |
| ($C_L$ = 15 pF) | $t_{PHL}$ | | |
| Input Capacitance | $C_{in}$ | 3.5 | pF |
| Power Dissipation Capacitance* | $C_{PD}$ | 36 | pF |

*$C_{PD}$ is used to determine the dynamic power consumption, per inverter when:
$P_D = V_{CC}^2 f (C_{PD} + C_L)$ where f = input frequency
$C_L$ = output load capacitance
$V_{CC}$ = supply voltage

**SWITCHING CHARACTERISTICS ($C_L$ = 50 pF, Input $t_r$ = $t_f$ = 6 ns)**

| CHARACTERISTIC | | TEST CONDITION | LIMITS | | | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | |
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | $V_{CC}$ V | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay | $t_{PLH}$ | 2 | | 90 | | — | | 115 | | — | | 135 | | — | |
| Input to Output | $t_{PHL}$ | 4.5 | | 18 | | 20 | | 23 | | 25 | | 27 | | 30 | ns |
| (Fig. 1) | | 6 | | 15 | | — | | 20 | | — | | 23 | | — | |
| Transition Times | $t_{TLH}$ | 2 | | 75 | | — | | 95 | | — | | 110 | | — | |
| (Fig. 1) | $t_{THL}$ | 4.5 | | 15 | | 15 | | 19 | | 19 | | 22 | | 22 | ns |
| | | 6 | | 13 | | — | | 16 | | — | | 19 | | | |

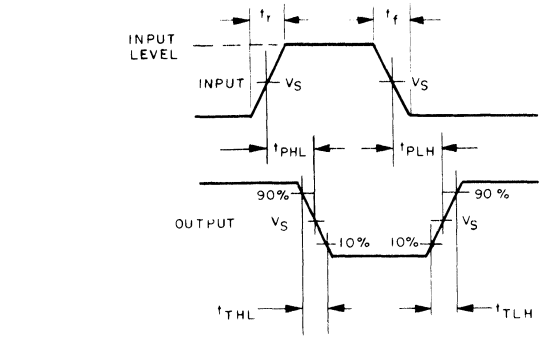
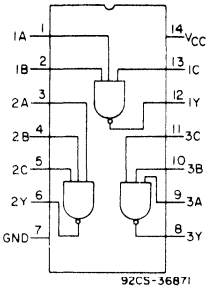



*Fig. 1 - Transition times and propagation delay times.*

**Preliminary Data** File Number **1475**




**TERMINAL ASSIGNMENT**

# Triple 3-Input AND Gate

**Type Features:**

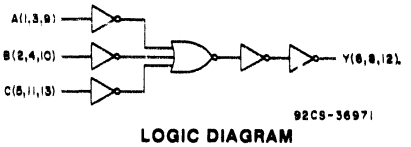
- *Buffered inputs*
- *Typical propagation delay = 11 ns@ $V_{CC}$ = 5V, $C_L$ = 15pF, TA=25°C*

**Family Features:**

- *Fanout [Over Temperature Range]:*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT/HCU: −40 to +85°C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Phillips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$=20%, $N_{IH}$=30% of $V_{CC}$; @ $V_{CC}$=5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$=0.8 V Max., $V_{IH}$=2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN}$, ≤ 1μA @ $V_{OL}$, $V_{OH}$*

The RCA-CD54/74HC11 and CD54/74HCT11 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC11 and CD54HCT11 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC11 and CD74HCT11 are supplied in 14-lead dual-in-line plastic packages (E suffix).




**LOGIC DIAGRAM**

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... −0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I$ <−0.5V or $V_I$ >$V_{CC}$ +0.5V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_o$ <−0.5V OR $V_o$ > $V_{CC}$ +0.5V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_o$) (FOR −0.5V < $V_o$ < $V_{CC}$ + 0.5V) ..... ±25 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±50 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to+85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For $T_A$ = −55 to +100°C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125°C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/°C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... −55 to +125°C
PACKAGE TYPE E ..... −40 to +85°C
STORAGE TEMPERATURE ($T_{stg}$) ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

**RECOMMENDED OPERATING CONDITIONS:**
**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$ = Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{in}$, $V_{out}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | −40 | +85 | °C |
| CD54 Types | −55 | +125 | °C |
| Input Rise and Fall Times $t_r$, $t_f$ | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC11/CD54HC11 | | | | | | | | | | CD74HCT11/CD54HCT11 | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC Series | | | 74HC Series | | 54HC Series | | TEST CONS. | | 74HCT/54HCT Series | | | 74HCT Series | | 54HCT Series | | |
| | | | | | | | -40/ | | -55/ | | | | | | | -40/ | | -55/ | | |
| | $V_{IN}$ | | $V_{CC}$ | +25°C | | | +85°C | | +125°C | | $V_{IN}$ | $V_{CC}$ | +25°C | | | +85°C | | +125°C | | |
| | V | | V | Min | Typ | Max | Min | Max | Min | Max | V | V | Min | Typ | Max | Min | Max | Min | Max | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | — | 4.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | 5.5 | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | — | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | 5.5 | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=−20μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | | | | | | | | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$(mA) −4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | −5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | | | | | | | | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$(mA) 4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V |
| | | 5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | | | | | | | | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 2 | — | 20 | — | 40 | $V_{CC}$ or Gnd | 5.5 | — | — | 2 | — | 20 | — | 40 | μA |

**SWITCHING CHARACTERISTICS ($C_L$=50 pF, Input $t_r$=$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25°C | | | | -40°C to +85°C | | | | -55°C to +125°C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay, Input to Output (Fig. 1) | $t_{PLH}$ | 2 | | 125 | | — | | 155 | | — | | 190 | | — | |
| | $t_{PHL}$ | 4.5 | | 25 | | 28 | | 31 | | 35 | | 38 | | 42 | ns |
| | | 6 | | 21 | | — | | 26 | | — | | 32 | | — | |
| Transition Times (Fig. 1) | $t_{TLH}$ | 2 | | 75 | | — | | 95 | | — | | 110 | | — | |
| | $t_{THL}$ | 4.5 | | 15 | | 15 | | 19 | | 19 | | 22 | | 22 | ns |
| | | 6 | | 13 | | — | | 16 | | — | | 19 | | — | |

**SWITCHING CHARACTERISTICS ($V_{CC}$=5 V, $T_A$=25°C, Input $t_r$=$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | 54/74HC/HCT | |
|---|---|---|---|
| | | Typical | Unit |
| Propagation Delay, Data Input to Output Y (Fig. 1) ($C_L$ = 15 pF) | $t_{PLH}$ $t_{PHL}$ | 11 | ns |
| Input Capacitance | $C_{IN}$ | 3.5 | pF |
| Power Dissipation Capacitance* | $C_{PD}$ | 35 | pF |

*$C_{PD}$ is used to determine the dynamic power consumption, per gate.

$PD = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where $f_i$ = input frequency

$f_o$ = output frequency

$c_L$ = output load capacitance

$V_{cc}$ = supply voltage

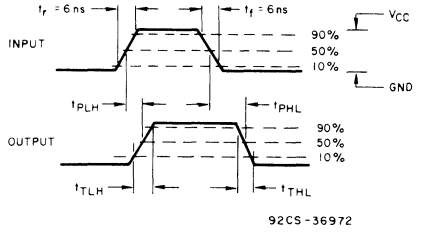
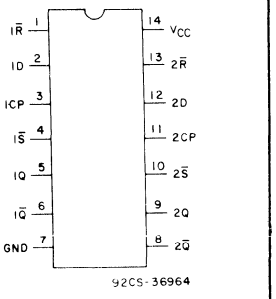



*Fig. 1 — Transition times and propagation delay times.*

| | 54/74HC | 54/74HCT |
|---|---|---|
| **Input Level** | $V_{CC}$ | 3V |
| $V_S$ | 50% $V_{CC}$ | 1.3V |

File Number **1476**

**Preliminary Data**




**TERMINAL ASSIGNMENT**

# Dual D Flip-Flop with SET and RESET Positive-Edge Trigger

**Type Features:**

- *Hysteresis on clock inputs for improved noise immunity and increased input Rise and Fall times.*
- *Asynchronous Set and Reset*
- *Compliment Outputs*
- *Buffered Inputs*
- *Typical $F_{max}$ = 50 MHz @ $V_{DD}$ − 5.0V, $C_L$ − 15 pF*

**Family Features:**

- *Fanout [Over Temperature Range]:*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT/HCU: −40 to +85° C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$=20%, $N_{IH}$=30% of $V_{CC}$; @ $V_{CC}$=5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$=0.8 V Max., $V_{IH}$=2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN}$, ≤ 1μA @ $V_{OL}$, $V_{OH}$*

The RCA-CD54/74HC74 and CD54/74HCT74 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL Loads.

This flip-flop has independent DATA, $\overline{SET}$, $\overline{RESET}$ and CLOCK inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. $\overline{SET}$ and $\overline{RESET}$ are independent of the clock and are accomplished by a low level at the appropriate input.

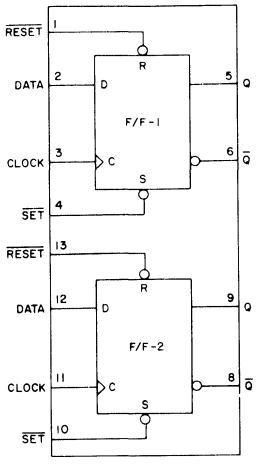
The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC74 and CD54HCT74 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC74 and CD74HCT74 are supplied in 14-lead dual-in-line plastic packages (E suffix).

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... 0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I$ < −0.5V or $V_I$ > $V_{CC}$ +0.5V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_o$ < −0.5V OR $V_o$ > $V_{CC}$ +0.5V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_o$) (FOR −0.5V < $V_o$ < $V_{CC}$ + 0.5V) ..... ±25 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±50 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = −40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = −55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... 55 to +125° C
PACKAGE TYPE E ..... 40 to +85° C
STORAGE TEMPERATURE ($T_{stg}$) ..... 65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

FUNCTIONAL DIAGRAM




$V_{CC}$ = PIN 14
GND = PIN 7
92CS-36965

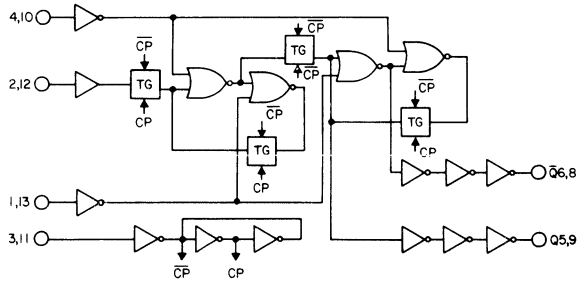
*Fig. 1 — Functional Diagram*

**TRUTH TABLE**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{SET}$ | $\overline{RESET}$ | CP | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H* | H* |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | Q0 | $\overline{Q0}$ |

H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
↑ = Transition from Low to High level

NOTES: QO = the level of Q before the indicated input conditions were established.
*This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.




LOGIC DIAGRAM 92CS-36966

*Fig. 2 — Logic Diagram*

**RECOMMENDED OPERATING CONDITIONS:**
**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$ = Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{in}$, $V_{out}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | −40 | +85 | °C |
| CD54 Types | −55 | +125 | °C |
| Input Rise and Fall Times $t_r$, $t_f$• | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

•Applicable for all inputs except clock.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC74/CD54HC74 | | | | | | | | | | CD74HCT74/CD54HCT74 | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC Series | | | 74HC Series | | 54HC Series | | TEST CONS. | | 74HCT/54HCT Series | | | 74HCT Series | | 54HCT Series | | |
| | $V_{IN}$ V | | $V_{CC}$ V | +25°C Min | +25°C Typ | +25°C Max | −40/+85°C Min | −40/+85°C Max | −55/+125°C Min | −55/+125°C Max | $V_{IN}$ V | $V_{CC}$ V | +25°C Min | +25°C Typ | +25°C Max | −40/+85°C Min | −40/+85°C Max | −55/+125°C Min | −55/+125°C Max | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | — | 4.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | 5.5 | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | $I_O$=−20μA | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | — | 4.5 | | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | 5.5 | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | — | — | — | — | — | — | — | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$(mA) −4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | −5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | — | — | — | — | — | — | | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | — | — | — | — | — | — | — | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | — | — | — | — | — | — | — | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$(mA) 4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V |
| | | 5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | — | — | — | — | — | — | | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 2 | — | 20 | — | 40 | $V_{CC}$ or Gnd | 5.5 | — | — | 2 | — | 20 | — | 40 | μA |

**SWITCHING CHARACTERISTICS ($C_L$=50 pF, Input $t_r$=$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25°C | | | | -40°C to +85°C | | | | -55°C to +125°C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay, | $t_{PLH}$ | 2 | | 175 | | — | | 220 | | — | | 265 | | — | |
| CP to Q, $\overline{Q}$ | $t_{PHL}$ | 4.5 | | 35 | | 35 | | 44 | | 44 | | 53 | | 53 | ns |
| (Fig. 3) | | 6 | | 30 | | — | | 37 | | — | | 45 | | — | |
| $\overline{R}$, $\overline{S}$ to Q, $\overline{Q}$ | $t_{PLH}$ | 2 | | 200 | | — | | 250 | | — | | 300 | | — | |
| (Fig. 4) | $t_{PHL}$ | 4.5 | | 40 | | 40 | | 50 | | 50 | | 60 | | 60 | ns |
| | | 6 | | 34 | | — | | 43 | | — | | 51 | | — | |
| Set-up Time | $t_{SU}$ | 2 | 100 | | — | | 125 | | — | | 150 | | — | | |
| (Data to CP) | | 4.5 | 20 | | 20 | | 25 | | 25 | | 30 | | 30 | | ns |
| (Fig. 3) | | 6 | 17 | | — | | 21 | | — | | 26 | | — | | |
| Hold Time | $t_H$ | 2 | 3 | | — | | 3 | | — | | 3 | | — | | |
| | | 4.5 | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| (Fig. 3) | | 6 | 3 | | — | | 3 | | — | | 3 | | — | | |
| Removal Time | $t_{REM}$ | 2 | 30 | | — | | 40 | | — | | 45 | | — | | |
| ($\overline{R}$, $\overline{S}$ to CP) | | 4.5 | 6 | | 6 | | 8 | | 8 | | 9 | | 9 | | ns |
| (Fig. 4) | | 6 | 5 | | — | | 7 | | — | | 8 | | — | | |
| Pulse Width | $t_W$ | 2 | 80 | | — | | 100 | | — | | 120 | | — | | |
| (CP, $\overline{R}$, $\overline{S}$) | | 4.5 | 16 | | 20 | | 20 | | 25 | | 24 | | 30 | | ns |
| (Fig. 3,4) | | 6 | 14 | | — | | 17 | | — | | 20 | | — | | |
| CP Frequency | $f_{MAX}$ | 2 | 6 | | — | | 5 | | — | | 4 | | — | | |
| | | 4.5 | 30 | | 25 | | 25 | | 20 | | 20 | | 16 | | MHz |
| | | 6 | 35 | | — | | 29 | | — | | 23 | | — | | |
| Transition Times | $t_{TLH}$ | 2 | | 75 | | — | | 95 | | — | | 110 | | — | |
| | $t_{THL}$ | 4.5 | | 15 | | 15 | | 19 | | 19 | | 22 | | 22 | ns |
| (Fig. 6) | | 6 | | 13 | | — | | 16 | | — | | 19 | | — | |

**SWITCHING CHARACTERISTICS ($V_{CC}$=5 V, $T_A$=25°C, Input $t_r$=$t_f$=6 ns)**

| CHARACTERISTICS | SYMBOL | 54/74HC/HCT | |
|---|---|---|---|
| | | Typical | Unit |
| Propagation Delay, CP to Q, $\overline{Q}$ ($C_L$ = 15 pF) | $t_{PLH}$ | | |
| ($C_L$ = 15 pF) (Fig. 3) | $t_{PHL}$ | 14 | ns |
| $\overline{R}$, $\overline{S}$ to Q, $\overline{Q}$ ($C_L$ = 15 pF) | $t_{PLH}$ | | |
| (Fig. 4) | $t_{PHL}$ | 17 | ns |
| CP Frequency ($C_L$ = 15 pF) | $f_{MAX}$ | 50 | Mhz |
| Input Capacitance | $C_{IN}$ | 3.5 | pF |
| Power Dissipation Capacitance* | $C_{PD}$ | 30 | pF |

*$C_{PD}$ is used to determine the dynamic power consumption, per flip-flop.

$PD = C_{PD} V_{CC}^2 fi + \Sigma C_L V_{CC}^2 fo$ where $f_i$ = input frequency

$f_o$ = output frequency

$c_L$ = output load capacitance

$V_{cc}$ = supply voltage

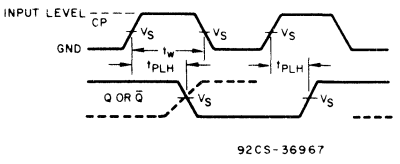



*Fig. 3 — Clock pre-requisite and propagation delays.*

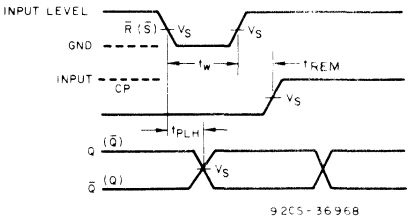



*Fig. 4 — $\overline{Reset}$ or $\overline{Set}$ pre-requisite and propagation delays.*

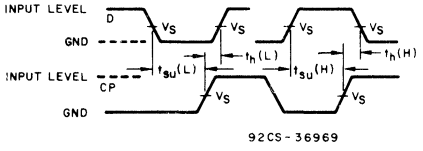



*Fig. 5 — Date pre-requisite times.*

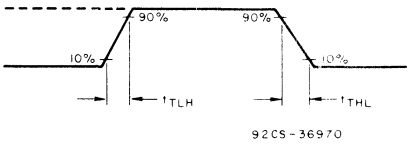
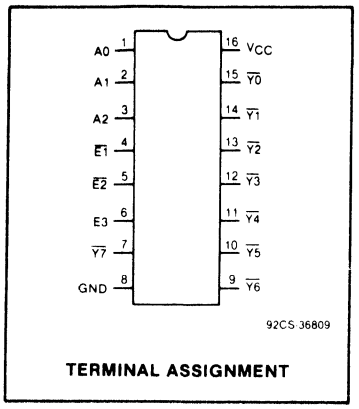



*Fig. 6 — Output transition times.*

| | 54/74HC | 54/74HCT |
|---|---|---|
| **Input Level** | **$V_{CC}$** | **3V** |
| $V_S$ | 50% $V_{CC}$ | 1.3V |

**Preliminary Data**

File Number **1477**




**TERMINAL ASSIGNMENT**

# 3-to-8 Line Decoder/Demultiplexer Inverting and Non-Inverting

**Type Features:**

- *Select one of eight data output [active LOW for 138, active HIGH for 238]*
- *I/O port or memory selector*
- *3 Enable Inputs to simplify cascading*
- *Typical propagation delay of 13ns @ $V_{CC}$ = 5V, 15pF, +25°C*

**Family Features:**

- *Fanout [Over Temperature Range]:*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT/HCU: -40 to +85°C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$=20%, $N_{IH}$=30% of $V_{CC}$; @ $V_{CC}$=5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$=0.8 V Max., $V_{IH}$=2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN}$ ≤ 1μA @ $V_{OL}$, $V_{OH}$*

The RCA-CD54/74HC138,238 and CD54/74HCT138,238 are high speed silicon gate CMOS decoders, and are well suited to memory address decoding or data routing applications. Both circuits feature low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic. Both circuits have 3 binary select inputs ($A_0$,$A_1$, and $A_2$). If the device is enabled these inputs determine which one of the eight normally high outputs of the HC/HCT138 series will go low or which of the normally low outputs of the HC/HCT238 series will go high.

Two active low and one active high enables ($\overline{E}_1$, $\overline{E}_2$, and $E_3$) are provided to ease the cascading of decoders. The decoder's outputs can drive 10 low power Schottky TTL equivalent loads.

The CD54HC138,238 and CD54HCT138,238 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC138,238 and CD74HCT138,238 are supplied in 16-lead dual-in-line plastic packages (E suffix).

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I$ <-0.5V or $V_I$ >$V_{CC}$ +0.5V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_O$ <-0.5V OR $V_O$ > $V_{CC}$ +0.5V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR -0.5V < $V_O$ < $V_{CC}$ + 0.5V) ..... ±25 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±50 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For $T_A$ = -55 to +100°C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125°C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/°C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

**RECOMMENDED OPERATING CONDITIONS:**
**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$ = Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{in}$, $V_{out}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | −40 | +85 | °C |
| CD54 Types | −55 | +125 | °C |
| Input Rise and Fall Times $t_r$, $t_f$ | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC138/238/CD54HC138/238 | | | | | | | | | | CD74HCT138/238/CD54HCT138/238 | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC Series | | | 74HC Series | | 54HC Series | | TEST CONS. | | 74HCT/54HCT Series | | | 74HCT Series | | 54HCT Series | | | |
| | $V_{IN}$ V | | $V_{CC}$ V | +25°C Min | +25°C Typ | +25°C Max | -40/+85°C Min | -40/+85°C Max | -55/+125°C Min | -55/+125°C Max | $V_{IN}$ V | $V_{CC}$ V | +25°C Min | +25°C Typ | +25°C Max | -40/+85°C Min | -40/+85°C Max | -55/+125°C Min | -55/+125°C Max | | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | — | 4.5 | 2 | — | — | 2 | — | 2 | — | | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | 5.5 | | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | — | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | 5.5 | | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=−20μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | | | | | | | | | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$(mA) −4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | | V |
| | | −5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | | | | | | | | | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$(mA) 4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | | V |
| | | 5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | | | | | | | | | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 8 | — | 80 | — | 160 | $V_{CC}$ or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | | μA |

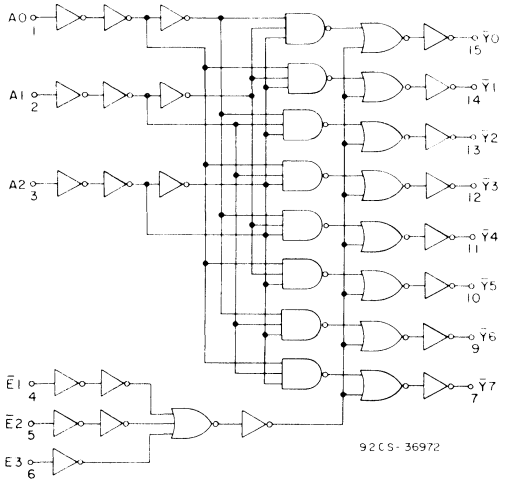



*Fig. 1 — Logic Diagram for HC/HCT 138*

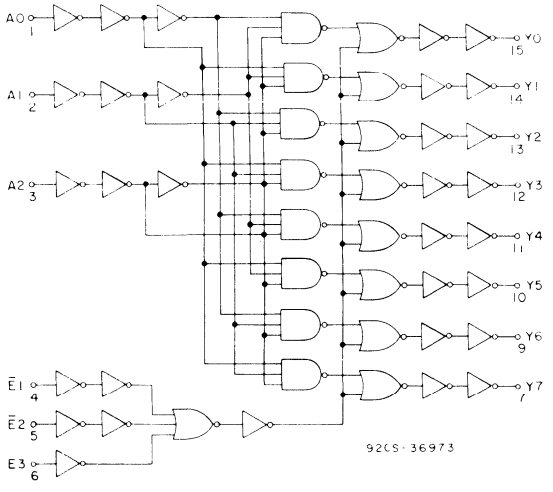



*Fig. 2 — Logic Diagram for HC/HCT 238*

**SWITCHING CHARACTERISTICS ($C_L$=50 pF, Input $t_r$=$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25°C | | | | -40°C to +85°C | | | | -55°C to +125°C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay, Address to Output (Fig. 3) | $t_{PLH}$ | 2 | | 150 | | — | | 190 | | — | | 225 | | — | ns |
| | $t_{PHL}$ | 4.5 | | 30 | | 35 | | 38 | | 44 | | 45 | | 53 | |
| | | 6 | | 26 | | — | | 33 | | — | | 38 | | — | |
| Propagation Delay, Enable Output (Fig. 4) | $t_{PLH}$ | 2 | | 175 | | — | | 220 | | — | | 265 | | — | ns |
| | $t_{PHL}$ | 4.5 | | 35 | | 40 | | 44 | | 50 | | 53 | | 60 | |
| | | 6 | | 30 | | — | | 37 | | — | | 45 | | — | |
| Transition Times (Fig. 3) | $t_{TLH}$ | 2 | | 75 | | — | | 95 | | — | | 110 | | — | ns |
| | $t_{THL}$ | 4.5 | | 15 | | 15 | | 19 | | 19 | | 22 | | 22 | |
| | | 6 | | 13 | | — | | 16 | | — | | 19 | | — | |

**SWITCHING CHARACTERISTICS ($V_{CC}$=5 V, $T_A$=25°C, $C_L$ = 15 pF, Input $t_r$=$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | 54/74HC/HCT | |
|---|---|---|---|
| | | Typical | Unit |
| Propagation Delay, Address to Output Y ($C_L$=15 pF) (Fig. 3) | $t_{PLH}$ $t_{PHL}$ | 13 | ns |
| Capacitance (Power Dissipation) | *$C_{PD}$ | 30 | pF |
| Input Capacitance | $C_{IN}$ | 3.5 | pF |

*$C_{PD}$ is used to determine the dynamic power consumption, per gate.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where $f_i$ = input frequency

$f_o$ = output frequency

$C_L$ = output load capacitance

$V_{CC}$ = supply voltage

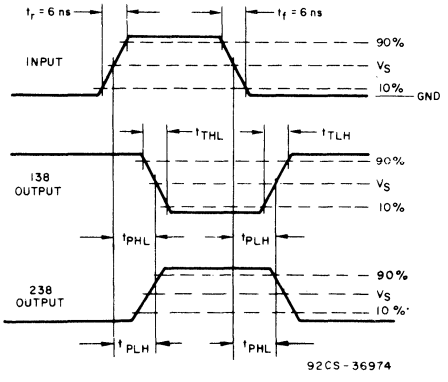



*Fig. 3 — Transition times and propagation delay times.*

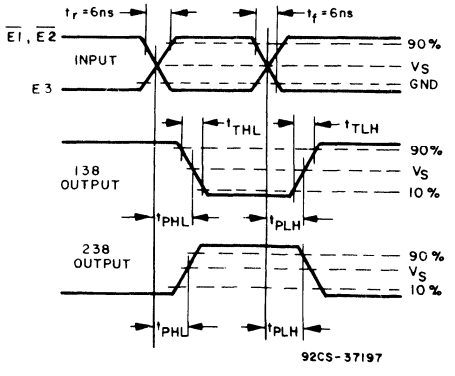



*Fig. 4 — Transitional times and propagation delay times.*

| Input Level | 54/74HC $V_{CC}$ | 54/74HCT 3V |
|---|---|---|
| $V_S$ | 50% $V_{CC}$ | 1.3V |

| Input Level | 54/74HC $V_{CC}$ | 54/74HCT 3V |
|---|---|---|
| $V_S$ | 50% $V_{CC}$ | 1.3V |

**TRUTH TABLE**
**CD54/74HC138,CD54/74HCT138**

| INPUTS | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ENABLE | | ADDRESS | | | | | | | | | | |
| $\overline{E}_3$ | $*\overline{E}_0$ | $A_2$ | $A_1$ | $A_0$ | $\overline{Y0}$ | $\overline{Y1}$ | $\overline{Y2}$ | $\overline{Y3}$ | $\overline{Y4}$ | $\overline{Y5}$ | $\overline{Y6}$ | $\overline{Y7}$ |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

H = High level, L = low level, X = don't care
$*\overline{E}_0 = \overline{E}_1 + \overline{E}_2$

**TRUTH TABLE**
**CD54/74HC238,CD54/74HCT238**

| INPUTS | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ENABLE | | ADDRESS | | | | | | | | | | |
| $\overline{E}_3$ | $*\overline{E}_0$ | $A_2$ | $A_1$ | $A_0$ | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | L | L | L | L | L | L | L | L |
| L | X | X | X | X | L | L | L | L | L | L | L | L |
| H | L | L | L | L | H | L | L | L | L | L | L | L |
| H | L | L | L | H | L | H | L | L | L | L | L | L |
| H | L | L | H | L | L | L | H | L | L | L | L | L |
| H | L | L | H | H | L | L | L | H | L | L | L | L |
| H | L | H | L | L | L | L | L | L | H | L | L | L |
| H | L | H | L | H | L | L | L | L | L | H | L | L |
| H | L | H | H | L | L | L | L | L | L | L | H | L |
| H | L | H | H | H | L | L | L | L | L | L | L | H |

H = High level, L = low level, X = don't care
$*\overline{E}_0 = \overline{E}_1 + \overline{E}_2$

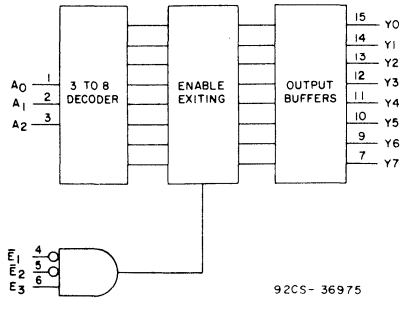
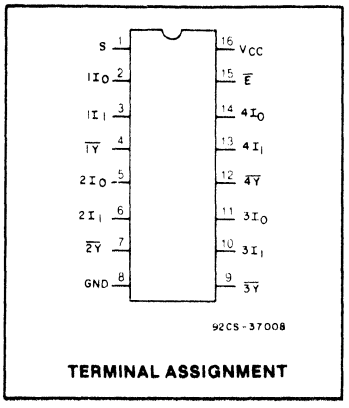



*Fig. 5 — Functional diagram for HC/HCT 138, 238.*

File Number **1481**

**Preliminary Data**




**TERMINAL ASSIGNMENT**

# Quad 2-Input Multiplexer; Inverting

**Type Features:**

- *Buffered inputs*
- *Typical Propagation Delay (In to Output)=12 ns @ $V_{CC}$=5 V, $C_L$=15 pF, $T_A$=25°C*

**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT/HCU: −40 to +85°C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*

The RCA-CD54/74HC158 and CD54/74HCT158 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When ($\overline{E}$) is HIGH, all of the outputs ($\overline{1Y}$-$\overline{4Y}$) are forced HIGH regardless of all other input conditions.

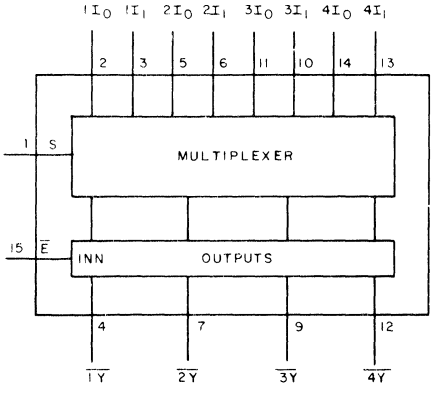
Moving data from two groups of registers to four common output busses is a common use of the 158. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator.

The CD54HC158 and CD54HCT158 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC158 and CD74HCT158 are supplied in 16-lead dual-in-line plastic packages (E suffix).

- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$=20%, $N_{IH}$=30% of $V_{CC}$, @ $V_{CC}$=5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$=0.8 V Max., $V_{IH}$=2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN} \leq 1\ \mu A$ @ $V_{OL}$, $V_{OH}$*

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR $-0.5\ V < V_o < V_{CC} + 0.5$ V) ..... ±25 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±50 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For $T_A$ = -55 to +100°C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125°C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/°C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C




PINNING

| | |
|---|---|
| S | SELECT INPUT |
| $I_0, I_1$ | MULTIPLEXER INPUTS |
| $\overline{Y}$ | OUTPUTS |
| $\overline{E}$ | OUTPUT ENABLE |

*Fig. 1 - Functional diagram.*

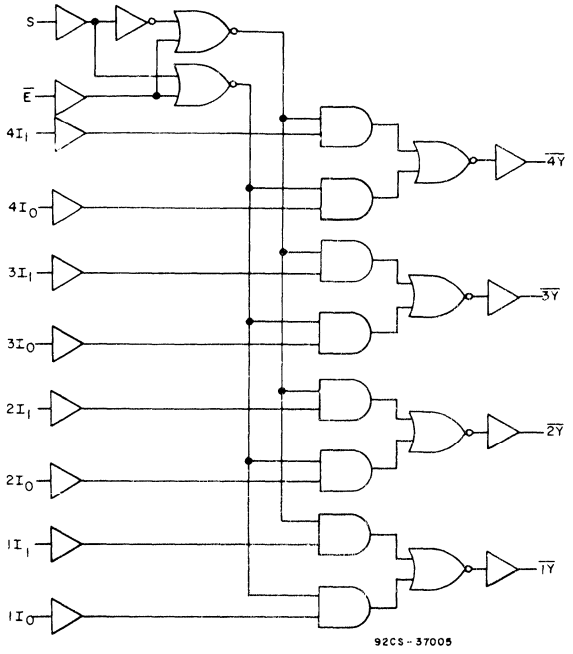



*Fig. 2 - Logic diagram.*

**FUNCTION TABLE**

| Enable | Select Input | Data Inputs | | Output |
|---|---|---|---|---|
| $\overline{E}$ | S | $I_0$ | $I_1$ | $\overline{Y}$ |
| H | X | X | X | H |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

**RECOMMENDED OPERATING CONDITIONS:**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$=Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{in}$, $V_{out}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times $t_r$,$t_f$ | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC158/CD54HC158 | | | | | | | | | | | CD74HCT158/CD54HCT158 | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC Series | | | 74HC Series | | 54HC Series | | | TEST CONS. | | 74HCT/54HCT Series | | | 74HCT Series | | 54HCT Series | | |
| | $V_{IN}$ V | | $V_{CC}$ V | +25°C Min | Typ | Max | -40/+85°C Min | Max | -55/+125°C Min | Max | | $V_{IN}$ V | $V_{CC}$ V | +25°C Min | Typ | Max | -40/+85°C Min | Max | -55/+125°C Min | Max | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | | — | 4.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | | 5.5 | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | | — | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | | 5.5 | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=-20μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | | — | — | — | — | — | — | — | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) -4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | -5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | | — | — | — | — | — | — | — | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | — | — | — | — | — | — | — | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | — | — | — | — | — | — | — | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) 4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V |
| | | 5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | | — | — | — | — | — | — | — | |
| Input Leakage Current $i_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 8 | — | 80 | — | 160 | | $V_{CC}$ or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | μA |

**SWITCHING CHARACTERISTICS ($V_{CC}$=5 V, $T_A$=25° C, Input $t_r$,$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | 54/74HC/HCT | |
|---|---|---|---|
| | | Typical | Units |
| In to $\overline{Y}$ ($C_L$ = 15 pF) | $t_{PHL}$ $t_{PLH}$ | 12 | ns |
| $\overline{E}$ to $\overline{Y}$ ($C_L$ = 15 pF) | $t_{PHL}$ $t_{PLH}$ | 13 | ns |
| S to $\overline{Y}$ ($C_L$ = 15 pF) | $t_{phl}$ $t_{plh}$ | 13 | ns |
| Input Capacitance | $C_{in}$ | 3.5 | pF |
| Power Dissipation Capacitance* | $C_{PD}$ | 35 | pF |

*$C_{PD}$ is used to determine the dynamic power consumption, per multiplexer.
PD = $C_{PD}$ $Vcc^2$ fi + Σ $C_L$ $Vcc^2$ fo where fi = input frequency
fo = output frequency
$C_L$ = output load capacitance
Vcc = supply voltage.

**SWITCHING CHARACTERISTICS ($C_L$=50 pF, Input $t_r$=$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay | $t_{PLH}$ | 2 | — | 140 | — | — | — | 175 | — | — | — | 210 | — | — | |
| In to $\overline{Y}$ | $t_{PHL}$ | 4.5 | — | 28 | — | 30 | — | 35 | — | 38 | — | 42 | — | 45 | ns |
| (Figure 3) | | 6 | — | 24 | — | — | — | 30 | — | — | — | 36 | — | — | |
| Propagation Delay | $t_{PLH}$ | 2 | — | 160 | — | — | — | 200 | — | — | — | 240 | — | — | |
| S to $\overline{Y}$ | $t_{PHL}$ | 4.5 | — | 32 | — | 35 | — | 40 | — | 44 | — | 48 | — | 53 | ns |
| (Figure 3) | | 6 | — | 27 | — | — | — | 34 | — | — | — | 41 | — | — | |
| Propagation Delay | $t_{PLH}$ | 2 | — | 150 | — | — | — | 190 | — | — | — | 225 | — | — | |
| $\overline{E}$ to $\overline{Y}$ | $t_{PHL}$ | 4.5 | — | 30 | — | 35 | — | 38 | — | 44 | — | 45 | — | 53 | ns |
| (Figure 4) | | 6 | — | 26 | — | — | — | 33 | — | — | — | 38 | — | — | |
| Output Transition | $t_{TLH}$ | 2 | — | 75 | — | — | — | 95 | — | — | — | 110 | — | — | |
| Time | $t_{THL}$ | 4.5 | — | 15 | — | 15 | — | 19 | — | 19 | — | 22 | — | 22 | ns |
| (Figure 3 or 4) | | 6 | — | 13 | — | — | — | 16 | — | — | — | 19 | — | — | |

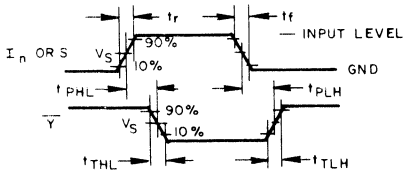
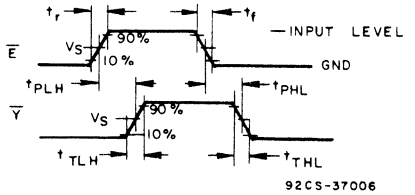



*Fig. 3 - Inputs or select to output propagation delays and output transition times.*

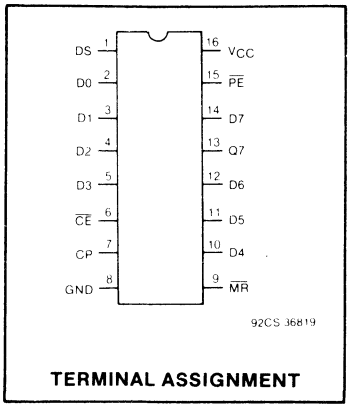



| INPUT LEVEL | 74/54 HC | 74/54 HCT |
|---|---|---|
| $V_S$ | 50% $V_{CC}$ | 1.3 V |

*Fig. 4 - Enable to output propagation delays and output transition times.*

File Number **1501**

**Preliminary Data**




**TERMINAL ASSIGNMENT**

# 8-Bit Parallel-In/Serial-Out Shift Register

**Type Features:**

- *Buffered inputs*
- *Typical $f_{max}$ = 50 MHz @ $V_{CC}$ = 5.0 V, $C_L$ = 15 pF, $T_A$ = 25° C*

**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT/HCU: -40 to +85° C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$ = 20%, $N_{IH}$ = 30% of $V_{CC}$; @ $V_{CC}$ = 5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$ = 0.8 V Max., $V_{IH}$ = 2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN} \leq 1\ \mu A$ @ $V_{OL}$, $V_{OH}$*

The RCA-CD54/74HC166 and CD54/74HCT166 8-bit shift register is fabricated with silicon gate CMOS technology. It possesses the low power consumption of standard CMOS integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky device.

The CD54/74HCT166 is functionally as well as pin compatible with the standard 54LS/74LS166.

The 166 is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ is LOW one setup time before the LOW-to-HIGH clock transition, parallel data is entered into the register. When $\overline{PE}$ is HIGH, data is entered into internal bit position $Q_0$ from Serial Data Input ($D_S$), and the remaining bits are shifted one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the $Q_7$ output is connected to the $D_S$ input of the succeeding stage.

The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for predictable operation.

A LOW on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

The CD54HC166 and CD54HCT166 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC166 and CD74HCT166 are supplied in 16-lead dual-in-line plastic packages (E suffix).

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR -0.5 V < $V_O$ < $V_{CC}$ +0.5 V) ..... ±25 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±50 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = -55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

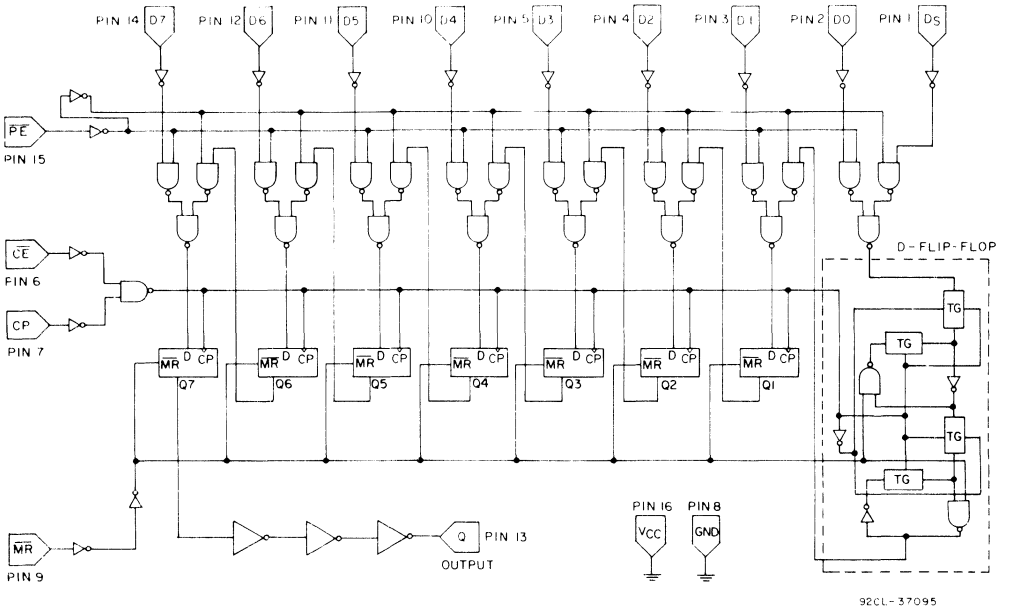



*Fig. 1 - Logic diagram.*

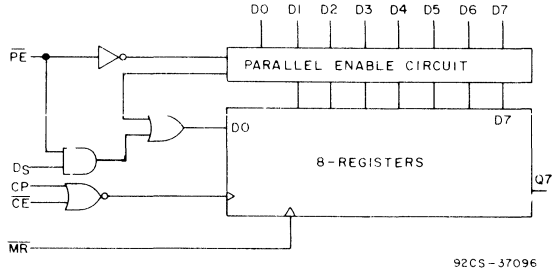



*Fig. 2 - Functional diagram.*

**TRUTH TABLE**

| Inputs | | | | | | Internal Outputs | | Output |
|---|---|---|---|---|---|---|---|---|
| Master Reset | Parallel Enable | Clock Enable | Clock | Serial | Parallel D0 D7 | Q0 | Q1 | QH |
| L | X | X | X | X | X | L | L | L |
| H | X | L | L | X | X | $Q_{00}$ | $Q_{10}$ | $Q_0$ |
| H | L | L | ↑ | X | a . . . h | a | b | h |
| H | H | L | ↑ | H | X | H | $Q_{0n}$ | $Q_{6n}$ |
| H | H | L | ↑ | L | X | L | $Q_{0n}$ | $Q_{6n}$ |
| H | X | H | ↑ | X | X | $Q_{00}$ | $Q_{10}$ | $Q_{70}$ |

H = high level (steady state).
L = low level (steady state).
X = irrelevant (any input, including transitions).
↑ = transition from low to high level.
a . . . h = the level of steady-state input at inputs D0 thru D7, respectively.
$Q_{00}$, $Q_{10}$, $Q_{70}$ = the level of $Q_0$, $Q_1$, or $Q_7$, respectively, before the indicated steady-state input conditions were established.
$Q_{0n}$, $Q_{6n}$ = the level of $Q_0$ or $Q_6$, respectively, before the most recent ↑ transition of the clock.

**RECOMMENDED OPERATING CONDITIONS:**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply Voltage Range (For $T_A$ = Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{IN}$, $V_{OUT}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times, tr, tf | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC166/CD54HC166 | | | | | | | | | | | CD74HCT166/CD54HCT166 | | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC Series | | | 74HC Series | | 54HC Series | | | TEST COND. | | 74HCT/54HCT Series | | | 74HCT Series | | 54HCT Series | | | | |
| | $V_{IN}$ V | | $V_{CC}$ V | +25°C Min | +25°C Typ | +25°C Max | -40/+85°C Min | -40/+85°C Max | -55/+125°C Min | -55/+125°C Max | | $V_{IN}$ V | $V_{CC}$ V | +25°C Min | +25°C Typ | +25°C Max | -40/+85°C Min | -40/+85°C Max | -55/+125°C Min | -55/+125°C Max | | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | | | 4.5 | 2 | — | — | 2 | — | 2 | — | | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | | 5.5 | | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | | | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | | 5.5 | | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=-20μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | | — | — | — | — | — | — | — | | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) -4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | | V |
| | | -5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | | — | — | — | — | — | — | — | | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | | | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | — | — | — | — | — | — | — | | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) 4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | | V |
| | | 5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | | — | — | — | — | — | — | — | | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 8 | — | 80 | — | 160 | | $V_{CC}$ or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | | μA |

**PRE-REQUISITE FOR SWITCHING FUNCTION**

| CHARACTERISTIC | | TEST CONDITION Vcc V | LIMITS 25°C HC Min. | HC Max. | HCT Min. | HCT Max. | -40°C to +85°C 74HC Min. | 74HC Max. | 74HCT Min. | 74HCT Max. | -55°C to +125°C 54HC Min. | 54HC Max. | 54HCT Min. | 54HCT Max. | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clock Frequency | $f_{max}$ | 2 | 6 | | — | | 5 | | — | | 4 | | — | | |
| Fig. 3 | | 4.5 | 30 | | 25 | | 25 | | 20 | | 20 | | 16 | | MHz |
| | | 6 | 35 | | — | | 29 | | — | | 23 | | — | | |
| $\overline{MR}$ Pulse Width | $t_w$ | 2 | 125 | | — | | 155 | | — | | 190 | | — | | |
| Fig. 4 | | 4.5 | 25 | | 35 | | 31 | | 44 | | 38 | | 53 | | ns |
| | | 6 | 22 | | — | | 26 | | — | | 32 | | — | | |
| Clock Pulse Width | $t_w$ | 2 | 80 | | — | | 100 | | — | | 120 | | — | | |
| Fig. 3 | | 4.5 | 16 | | 20 | | 20 | | 25 | | 24 | | 30 | | ns |
| | | 6 | 14 | | — | | 17 | | — | | 20 | | — | | |
| Set-up Time | $t_{su}$ | 2 | 100 | | — | | 125 | | — | | 150 | | — | | |
| Data and $\overline{CE}$ to | | 4.5 | 20 | | 20 | | 25 | | 25 | | 30 | | 30 | | ns |
| Clock, Fig. 5, 6 | | 6 | 17 | | — | | 21 | | — | | 26 | | — | | |
| Hold Time | $t_H$ | 2 | 0 | | — | | 0 | | — | | 0 | | — | | |
| Data and $\overline{CE}$ to | | 4.5 | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Clock, Fig. 5 | | 6 | 0 | | — | | 0 | | — | | 0 | | — | | |
| Removal Time | $t_{REM}$ | 2 | 0 | | — | | 0 | | — | | 0 | | — | | |
| $\overline{MR}$ to Clock | | 4.5 | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Fig. 4 | | 6 | 0 | | — | | 0 | | — | | 0 | | — | | |
| Set-up Time | $t_{su}$ | 2 | 150 | | — | | 190 | | — | | 225 | | — | | |
| $\overline{PE}$ to CP | | 4.5 | 30 | | 30 | | 38 | | 38 | | 45 | | 45 | | ns |
| Fig. 6 | | 6 | 26 | | — | | 33 | | — | | 38 | | — | | |
| Hold Time | $t_H$ | 2 | 0 | | — | | 0 | | — | | 0 | | — | | |
| $\overline{PE}$ to CP | | 4.5 | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Fig. 6 | | 6 | 0 | | — | | 0 | | — | | 0 | | — | | |

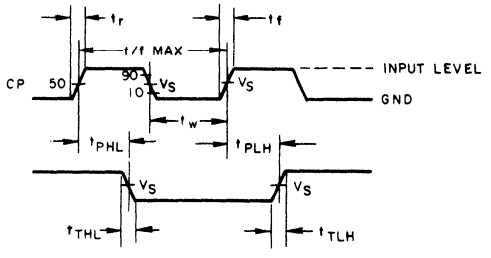
**SWITCHING CHARACTERISTICS ($C_L$ = 50 pF, Input $t_r$ = $t_f$ = 6 ns)**

| CHARACTERISTIC | | TEST CONDITION Vcc V | LIMITS 25°C HC Min. | HC Max. | HCT Min. | HCT Max. | -40°C to +85°C 74HC Min. | 74HC Max. | 74HCT Min. | 74HCT Max. | -55°C to +125°C 54HC Min. | 54HC Max. | 54HCT Min. | 54HCT Max. | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Propagation Delay | $t_{PLH}$ | 2 | | 175 | | — | | 220 | | — | | 265 | | — | |
| Clock to Output | $t_{plh}$ | 4.5 | | 35 | | 40 | | 44 | | 50 | | 53 | | 60 | ns |
| Fig. 3 | | 6 | | 30 | | — | | 37 | | — | | 45 | | — | |
| Output Transition | $t_{TLH}$ | 2 | | 75 | | — | | 95 | | — | | 110 | | — | |
| Time | $t_{THL}$ | 4.5 | | 15 | | 15 | | 19 | | 19 | | 22 | | 22 | ns |
| Fig. 3 | | 6 | | 13 | | — | | 16 | | — | | 19 | | — | |
| Propagation Delay | $t_{PHL}$ | 2 | | 200 | | — | | 250 | | — | | 300 | | — | |
| $\overline{MR}$ to Output | | 4.5 | | 40 | | 45 | | 50 | | 56 | | 60 | | 68 | ns |
| Fig. 4 | | 6 | | 34 | | — | | 43 | | — | | 51 | | — | |

**SWITCHING CHARACTERISTICS (Vcc = 5 V, TA = 25° C, Input tr = tf = 6 ns)**

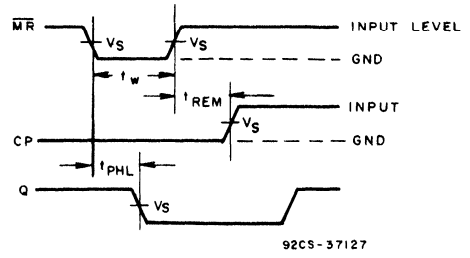
| CHARACTERISTIC | | 54/74HC/HCT TYPICAL | UNIT |
|---|---|---|---|
| Propagation Delay, ($C_L$ = 15 pF) Clock to Q | tPLH tPHL | 15 | ns |
| Maximum Clock Frequency ($C_L$ = 15 pF) | fmax | 50 | MHz |
| Input Capacitance | Cin | 3.5 | pF |
| Power Dissipation Capacitance* | CPD | 25 | pF |

*CPD is used to determine the dynamic power consumption, per function.



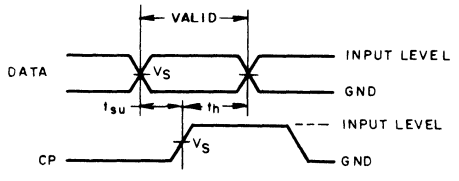

| Input Level VS | 54/74HC $V_{CC}$ | 54/74HC $50\%\ V_{CC}$ | 54/74HCT 3.0 V | 54/74HCT 1.3 V |
|---|---|---|---|---|

*Fig. 3 - Clock pre-requisite times and propagation and output transition times.*



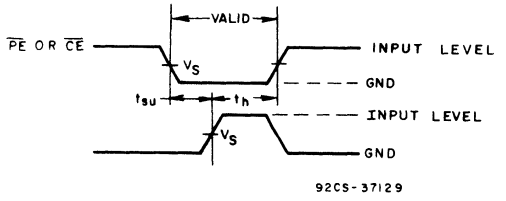

| Input Level VS | 54/74HC $V_{CC}$ | 54/74HC $50\%\ V_{CC}$ | 54/74HCT 3.0 V | 54/74HCT 1.3 V |
|---|---|---|---|---|

*Fig. 4 - Master reset pre-requisite times and propagation delays.*




| Input Level VS | 54/74HC $V_{CC}$ | 54/74HC $50\%\ V_{CC}$ | 54/74HCT 3.0 V | 54/74HCT 1.3 V |
|---|---|---|---|---|

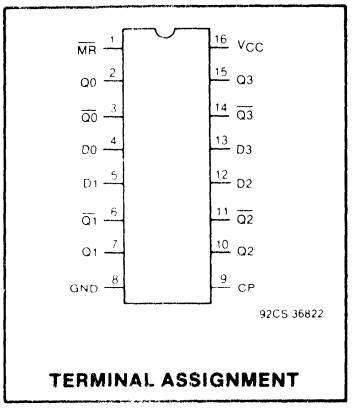
*Fig. 5 - Data pre-requisite times.*




| Input Level VS | 54/74HC $V_{CC}$ | 54/74HC $50\%\ V_{CC}$ | 54/74HCT 3.0 V | 54/74HCT 1.3 V |
|---|---|---|---|---|

*Fig. 6 - Parallel enable or clock enable pre-requisite times.*

**Preliminary Data** File Number **1474**




**TERMINAL ASSIGNMENT**

# Quad D Flip-Flop with Reset

**Type Features:**

- *Common Clock and Asynchronous Reset on four D-Type Flip-Flops*
- *Positive edge-pulse triggering*
- *Complement Outputs*
- *Buffered Inputs*
- *Typical $F_{max}$ = 50 MHz @ $V_{CC}$ = 5.0 V, $C_L$ = 15 pF, $T_A$ = 25° C*

**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$ = 20%, $N_{IH}$ = 30% of $V_{CC}$; @ $V_{CC}$ = 5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$ = 0.8 V Max., $V_{IH}$ = 2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN} \leq 1\ \mu A$ @ $V_{OL}$, $V_{OH}$*

The RCA CD54/74HC175 and the CD54/74HCT175 are high speed Quad D-Type Flip-Flops with individual D-inputs and Q, $\overline{Q}$ complementary outputs. The devices are fabricated using silicon gate CMOS technology. They have the low power consumption advantage of standard CMOS ICs and the ability to drive 10 LSTTL devices.

Information at the D input is transferred to the Q and $\overline{Q}$ outputs on the positive-going edge of the clock pulse. All four Flip-Flops are controlled by a common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock. All four Q outputs are reset to a logic 0 and all four $\overline{Q}$ outputs to a logic 1.

The CD54HC175 and CD54HCT175 are supplied in 16-lead dual-in-line ceramic packages (F-suffix) and the CD74HC175 and CD74HCT175 are supplied in 16-lead dual-in-line plastic packages (E-suffix).

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR -0.5 V < $V_O$ < $V_{CC}$ +0.5 V) ..... ±25 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±50 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = -55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

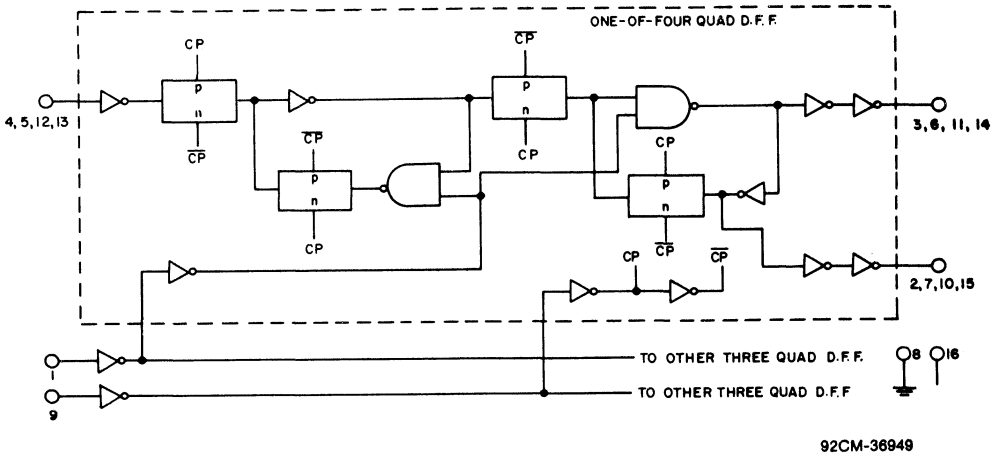



*Fig. 1 - Logic block diagram.*

**TRUTH TABLE**
**(EACH FLIP-FLOP)**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| RESET ($\overline{MR}$) | CLOCK CP | DATA Dn | Qn | $\overline{Qn}$ |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | Qo | $\overline{Qo}$ |

H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
↑ = Transition from Low to High Level
Qo, $\overline{Qo}$ = Levels Before the Indicated Steady-State Input Conditions were Established

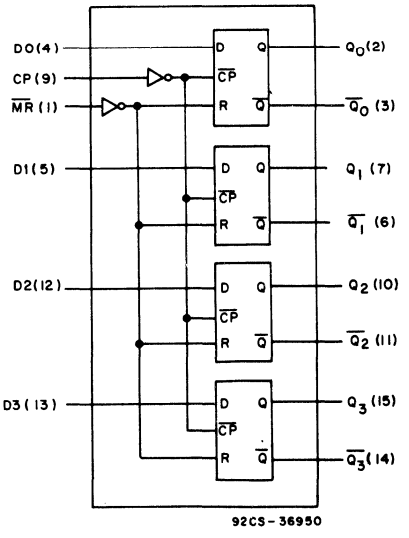



*Fig. 2 - Functional diagram.*

**RECOMMENDED OPERATING CONDITIONS:**

**For maximum reliability, nominal conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply Voltage Range (For $T_A$ = Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{IN}$, $V_{OUT}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times, $t_r$, $t_f$ | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC175/CD54HC175 | | | | | | | | | | | CD74HCT175/CD54HCT175 | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC Series | | | 74HC Series | | 54HC Series | | | TEST COND. | | 74HCT/54HCT Series | | | 74HCT Series | | 54HCT Series | | |
| | | | | +25°C | | | -40/ +85°C | | -55/ +125°C | | | | | +25°C | | | -40/ +85°C | | -55/ +125°C | | |
| | $V_{IN}$ V | | $V_{CC}$ V | Min | Typ | Max | Min | Max | Min | Max | | $V_{IN}$ V | $V_{CC}$ V | Min | Typ | Max | Min | Max | Min | Max | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | | | 4.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | | 5.5 | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | | | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | | 5.5 | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=-20μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | | — | — | — | — | — | — | — | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) -4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | -5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | | — | — | — | — | — | — | — | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | — | — | — | — | — | — | — | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) 4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V |
| | | 5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | | — | — | — | — | — | — | — | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 8 | — | 80 | — | 160 | | $V_{CC}$ or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | μA |

**PRE-REQUISITE FOR SWITCHING FUNCTION 54/74HC SERIES AND 54/74HCT SERIES**

| CHARACTERISTIC | TEST CONDITION | LIMITS | | | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 25°C | | | | -40°C to +85°C | | | | -55°C to +125°C | | | | |
| | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | Vcc V | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Clock Pulse | 2 | 80 | | | | 100 | | | | 120 | | | | |
| Width tw | 4.5 | 16 | | 20 | | 20 | | 25 | | 24 | | 30 | | ns |
| Fig. 3 | 6 | 14 | | | | 17 | | | | 20 | | | | |
| | 2 | 80 | | | | 100 | | | | 120 | | | | |
| $\overline{MR}$ Pulse Width tw | 4.5 | 16 | | 20 | | 20 | | 25 | | 24 | | 30 | | ns |
| Fig. 4 | 6 | 14 | | | | 17 | | | | 20 | | | | |
| Setup Time Data | 2 | 100 | | | | 125 | | | | 150 | | | | |
| to Clock tsu | 4.5 | 20 | | 20 | | 25 | | 25 | | 30 | | 30 | | ns |
| Fig. 5 | 6 | 17 | | | | 21 | | | | 26 | | | | |
| Hold Time Data | 2 | 5 | | | | 5 | | | | 5 | | | | |
| to Clock th | 4.5 | 5 | | 5 | | 5 | | 5 | | 5 | | 5 | | ns |
| Fig. 5 | 6 | 5 | | | | 5 | | | | 5 | | | | |
| Removal Time | 2 | 5 | | | | 5 | | | | 5 | | | | |
| $\overline{MR}$ to Clock trem | 4.5 | 5 | | 5 | | 5 | | 5 | | 5 | | 5 | | ns |
| Fig. 4 | 6 | 5 | | | | 5 | | | | 5 | | | | |

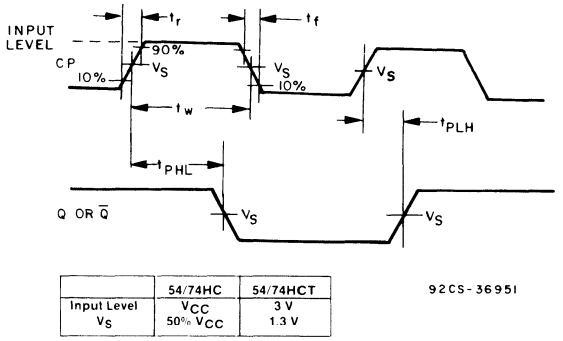
**SWITCHING CHARACTERISTICS ($C_L$ = 50 pF, Input $t_r$ = $t_f$ = 6 ns)**

| CHARACTERISTIC | TEST CONDITION | LIMITS | | | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 25°C | | | | -40°C to +85°C | | | | -55°C to +125°C | | | | |
| | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | Vcc V | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| | 2 | | 175 | | | | 220 | | | | 265 | | | |
| Propagation Delay tPLH | 4.5 | | 35 | | 35 | | 44 | | 44 | | 53 | | 53 | ns |
| Clock to Q or $\overline{Q}$ | 6 | | 30 | | | | 37 | | | | 45 | | | |
| Fig. 3 | 2 | | 175 | | | | 220 | | | | 265 | | | |
| tPHL | 4.5 | | 35 | | 35 | | 44 | | 44 | | 53 | | 53 | ns |
| | 6 | | 30 | | | | 37 | | | | 45 | | | |
| Propagation Delay tPLH | 2 | | 175 | | | | 220 | | | | 265 | | | |
| ($\overline{MR}$) to Q or $\overline{Q}$ tPHL | 4.5 | | 35 | | 35 | | 44 | | 44 | | 53 | | 53 | ns |
| Fig. 4 | 6 | | 30 | | | | 37 | | | | 45 | | | |
| | 2 | | 75 | | | | 95 | | | | 110 | | | |
| Output Transistion tTLH | 4.5 | | 15 | | 15 | | 19 | | 19 | | 22 | | 22 | ns |
| Time | 6 | | 13 | | | | 16 | | | | 19 | | | |
| Fig. 6 | 2 | | 75 | | | | 95 | | | | 110 | | | |
| tTHL | 4.5 | | 15 | | 15 | | 19 | | 19 | | 22 | | 22 | ns |
| | 6 | | 13 | | | | 16 | | | | 19 | | | |
| | 2 | 6 | | | | 5 | | | | 4 | | | | |
| Clock Frequency fmax | 4.5 | 30 | | 25 | | 25 | | 20 | | 20 | | 16 | | MHz |
| | 6 | 35 | | | | 29 | | | | 23 | | | | |

**SWITCHING CHARACTERISTICS ($V_{CC}$ = 5 V, $T_A$ = 25° C, $C_L$ = 15 pF, Input $t_r$ = $t_f$ = 6 ns)**

| CHARACTERISTIC | | 54/74HC/HCT TYPICAL | UNIT |
|---|---|---|---|
| Propagation Delay- Clock to Q or $\overline{Q}$, Fig. 3 | $t_{PLH}$ $t_{PHL}$ | 14 | ns |
| Propagation Delay- $\overline{MR}$ to Q or $\overline{Q}$, Fig. 4 | $t_{PHL}$ $t_{PLH}$ | 14 | ns |
| Power Dissipation Capacitance | $C_{PD}$* | 65 | pF |
| Input Capacitance | $C_{in}$ | 3.5 | pF |

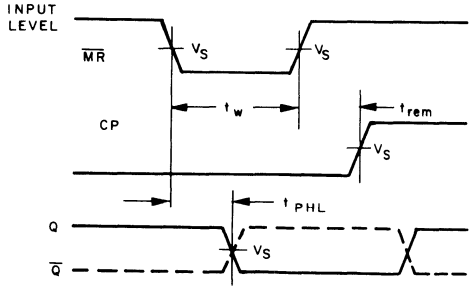
*$C_{PD}$ is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD}V_{CC}^2f_i + \Sigma\ C_LV_{CC}^2f_o$ where $f_i$ = input frequency, $f_o$ = output frequency,
$C_L$ = output load capacitance, $V_{CC}$ = supply voltage




| | 54/74HC | 54/74HCT |
|---|---|---|
| Input Level $V_S$ | $V_{CC}$ 50% $V_{CC}$ | 3 V 1.3 V |

92CS-36951

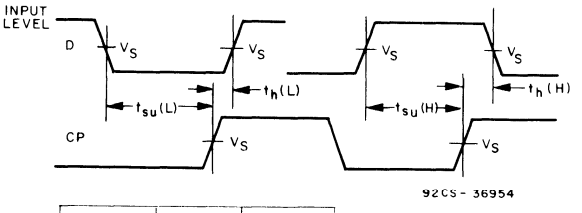
*Fig. 3 - Propagation delay times and clock pulse width.*




| | 54/74HC | 54/74HCT |
|---|---|---|
| Input Level $V_S$ | $V_{CC}$ 50% $V_{CC}$ | 3 V 1.3 V |

92CS-36952

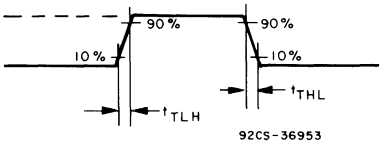
*Fig. 4 - Pre-requisite and propagation delay times for master reset.*




| | 54/74HC | 54/74HCT |
|---|---|---|
| Input Level $V_S$ | $V_{CC}$ 50% $V_{CC}$ | 3 V 1.3 V |

92CS-36954

*Fig. 5 - Pre-requisite for clock.*

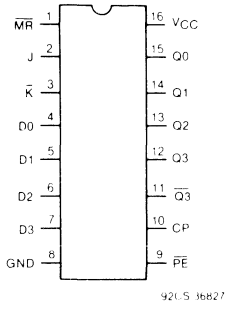



92CS-36953

*Fig. 6 - Transition times.*

File Number **1482**

**Preliminary Data**




**TERMINAL ASSIGNMENT**

# 4-Bit Parallel Access Register

**Type Features:**

- *Asynchronous Master Reset*
- *J, K, (D) inputs to first stage*
- *Fully synchronous serial or parallel data transfer*
- *Shift right and parallel load capability*
- *Complementary output from last stage*
- *Buffered inputs*
- *Typical $f_{MAX}$=50 MHz @ $V_{CC}$=5 V, $C_L$=15 pF, $T_A$=25°C*

**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT/HCU: −40 to +85°C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$=20%, $N_{IH}$=30% of $V_{CC}$; @ $V_{CC}$=5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$=0.8 V Max., $V_{IH}$=2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN} \leq 1\ \mu A$ @ $V_{OL}$, $V_{OH}$*

The functional characteristics of the RCA-CD54/74HC195 and CD54/74HCT195 4-Bit Parallel Access Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

The HC/HCT195 series operates in two primary modes: shift right (Q0-Q1) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is high, and is shifted one bit in the direction Q0-Q1-Q2-Q3 following each LOW-to-HIGH clock transition. The J and $\overline{K}$ inputs provide the flexibility of the JK-type input for special applications and, by tying the two pins together, the simple D-type input for general applications. The device appears as four common-clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (P0-P3) is transferred to the respective Q0-Q3 outputs. Shift left operation (Q3-Q2) can be achieved by tying the Qn outputs to the $D_{n-1}$ inputs and holding the $\overline{PE}$ input low.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The HC/HCT195 series utilizes edge-triggering; therefore, there is no restriction on the activity of the J, $\overline{K}$, $Pn_1$ and $\overline{PE}$ inputs for logic operations, other than the set-up and hold time requirements. A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

The CD54HC195 and CD54HCT195 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC195 and CD74HCT195 are supplied in 16-lead dual-in-line plastic packages (E suffix).

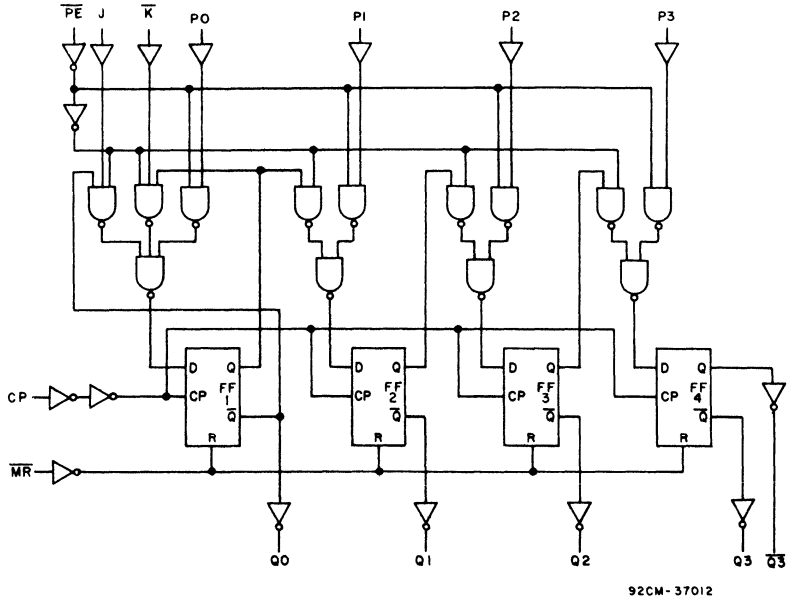
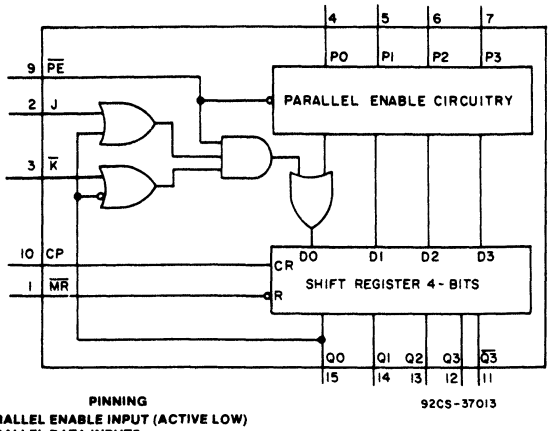



*Fig. 1 - Logic diagram.*

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR $-0.5$ V $< V_O <$ $V_{CC}$ + 0.5 V) ..... ±25 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±50 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = -55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C




**PINNING**

| | |
|---|---|
| PE | PARALLEL ENABLE INPUT (ACTIVE LOW) |
| D0 to D3 | PARALLEL DATA INPUTS |
| J | FIRST STAGE J-INPUT (ACTIVE HIGH) |
| K | FIRST STAGE K-INPUT (ACTIVE LOW) |
| CP | CLOCK INPUT (LOW-TO-HIGH EDGE TRIGGERED) |
| MR | MASTER RESET INPUT (ACTIVE LOW) |
| Q0-Q3 | BUFFERED PARALLEL OUTPUTS |
| Q3 | BUFFERED INVERTED OUTPUT FROM LAST STAGE |

*Fig. 2 - Function diagram.*

**Function Table**

| Operating Modes | INPUTS | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | $\overline{CP}$ | PE | J | $\overline{K}$ | $D_n$ | Q0 | Q1 | Q2 | Q3 | $\overline{Q3}$ |
| Asynchronous Reset | L | X | X | X | X | X | L | L | L | L | H |
| Shift, Set first stage | H | ↑ | h | h | h | X | H | $q_0$ | $q_1$ | $q_2$ | $\overline{q}_2$ |
| Shift, Reset first stage | H | ↑ | h | l | l | X | L | $q_0$ | $q_1$ | $q_2$ | $\overline{q}_2$ |
| Shift, Toggle first stage | H | ↑ | h | h | l | X | $\overline{q}_0$ | $q_0$ | $q_1$ | $q_2$ | $\overline{q}_2$ |
| Shift, Retain first stage | H | ↑ | h | l | h | X | $q_0$ | $q_0$ | $q_1$ | $q_2$ | $\overline{q}_2$ |
| Parallel Load | H | ↑ | l | X | X | $d_n$ | $d_0$ | $d_1$ | $d_2$ | $d_3$ | $\overline{d}_3$ |

H=HIGH voltage level.
L=LOW voltage level.
X=Don't care.
l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
$d_n$ ($q_n$)=Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.
↑=LOW-to-HIGH clock transition.

**RECOMMENDED OPERATING CONDITIONS:**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$=Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{in}$, $V_{out}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times $t_r$,$t_f$ | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC195/CD54HC195 | | | | | | | | | | CD74HCT195/CD54HCT195 | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC Series | | | 74HC Series | | 54HC Series | | TEST CONS. | | 74HCT/54HCT Series | | | 74HCT Series | | 54HCT Series | | | |
| | $V_{IN}$ | | $V_{CC}$ | +25°C | | | -40/ +85°C | | -55/ +125°C | | $V_{IN}$ | $V_{CC}$ | +25°C | | | -40/ +85°C | | -55/ +125°C | | | |
| | V | | V | Min | Typ | Max | Min | Max | Min | Max | V | V | Min | Typ | Max | Min | Max | Min | Max | | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | — | 4.5 | 2 | — | — | 2 | — | 2 | — | V | |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | 5.5 | | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | — | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V | |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | 5.5 | | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=-20μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V | |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | — | — | — | — | — | — | — | | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) -4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V | |
| | | -5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | — | — | — | — | — | — | — | | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20 μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | — | — | — | — | — | — | — | — | V | |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | — | — | — | — | — | — | — | | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) 4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | $V_{IL}$ or $V_{IH}$ | — | — | — | — | — | — | — | — | V | |
| | | 5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | | |
| | | | | | | | | | | | | | — | — | — | — | — | — | — | | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA | |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 8 | — | 80 | — | 160 | $V_{CC}$ or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | μA | |

**SWITCHING CHARACTERISTICS ($V_{CC}$=5 V, $T_A$=25° C, Input $t_r$,$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | 54/74HC/HCT | |
|---|---|---|---|
| | | Typical | Units |
| CP to $Q_n$ ($C_L$ = 15 pF) | $t_{PHL}$ $t_{PLH}$ | 14 | ns |
| $\overline{MR}$ to $Q_n$ ($C_L$ = 15 pF) | $t_{PHL}$ | 13 | ns |
| $f_{MAX}$ ($C_L$ = 15 pF) | $f_{MAX}$ | 50 | MHz |
| Input Capacitance | $C_{in}$ | 3.5 | pF |
| Power Dissipation Capacitance* | $C_{PD}$ | 48 | pF |

*$C_{PD}$ is used to determine the dynamic power consumption, per register.
$PD = C_{PD} Vcc^2 fi + \Sigma C_L Vcc^2 fo$ where
fi = input frequency
fo = output frequency
$C_L$ = output load capacitance
Vcc = supply voltage.

**Pre-requisite for Switching Function**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Clock Frequency | $f_{MAX}$ | 2 | 6 | — | — | — | 5 | — | — | — | 4 | — | — | — | |
| (Figure 3) | | 4.5 | 30 | — | 25 | — | 25 | — | 20 | — | 20 | — | 16 | — | ns |
| | | 6 | 35 | — | — | — | 29 | — | — | — | 23 | — | — | — | |
| $\overline{MR}$ Pulse Width | $t_w$ | 2 | 80 | — | — | — | 100 | — | — | — | 120 | — | — | — | |
| (Figure 3) | | 4.5 | 16 | — | 20 | — | 20 | — | 25 | — | 24 | — | 30 | — | ns |
| | | 6 | 14 | — | — | — | 17 | — | — | — | 20 | — | — | — | |
| Clock Pulse Width | $t_w$ | 2 | 80 | — | — | — | 100 | — | — | — | 120 | — | — | — | |
| (Figure 3) | | 4.5 | 16 | — | 20 | — | 20 | — | 25 | — | 24 | — | 30 | — | ns |
| | | 6 | 14 | — | — | — | 17 | — | — | — | 20 | — | — | — | |
| Set-up Time | $t_{SU}$ | 2 | 100 | — | — | — | 125 | — | — | — | 150 | — | — | — | |
| J, $\overline{K}$, $\overline{PE}$ to Clock | | 4.5 | 20 | — | 20 | — | 25 | — | 25 | — | 30 | — | 30 | — | ns |
| (Figure 5) | | 6 | 17 | — | — | — | 21 | — | — | — | 26 | — | — | — | |
| Hold Time | $t_h$ | 2 | 3 | — | — | — | 3 | — | — | — | 3 | — | — | — | |
| J, $\overline{K}$, $\overline{PE}$ to Clock | | 4.5 | 3 | — | 3 | — | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| (Figure 5) | | 6 | 3 | — | — | — | 3 | — | — | — | 3 | — | — | — | |
| Removal Time | $t_{REM}$ | 2 | 80 | — | — | — | 100 | — | — | — | 120 | — | — | — | |
| $\overline{MR}$ to Clock | | 4.5 | 16 | — | 16 | — | 20 | — | 20 | — | 24 | — | 24 | — | ns |
| (Figure 3) | | 6 | 14 | — | — | — | 17 | — | — | — | 20 | — | — | — | |

**SWITCHING CHARACTERISTICS ($C_L$=50 pF, Input $t_r$,$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay | $t_{PLH}$ | 2 | — | 175 | — | — | — | 220 | — | — | — | 265 | — | — | |
| CP to Output | $t_{PHL}$ | 4.5 | — | 35 | — | 35 | — | 44 | — | 44 | — | 53 | — | 53 | ns |
| (Figure 3) | | 6 | — | 30 | — | — | — | 37 | — | — | — | 45 | — | — | |
| Propagation Delay | $t_{PHL}$ | 2 | — | 150 | — | — | — | 190 | — | — | — | 225 | — | — | |
| $\overline{MR}$ to Output | $t_{PLH}$ | 4.5 | — | 30 | — | 35 | — | 38 | — | 44 | — | 45 | — | 53 | ns |
| (Figure 3) | | 6 | — | 26 | — | — | — | 33 | — | — | — | 38 | — | — | |
| Output Transition | $t_{TLH}$ | 2 | — | 75 | — | — | — | 95 | — | — | — | 110 | — | — | |
| Time | $t_{THL}$ | 4.5 | — | 15 | — | 15 | — | 19 | — | 19 | — | 22 | — | 22 | ns |
| | | 6 | — | 13 | — | — | — | 16 | — | — | — | 19 | — | — | |

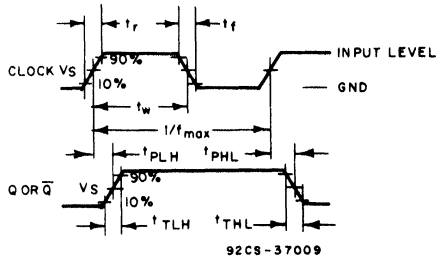



*Fig. 3 - Clock pre-requisite and propagation delays and output transition times.*

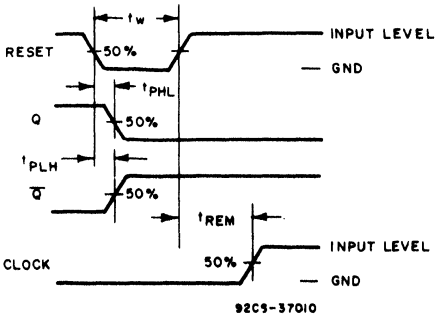



*Fig. 4 - Master Reset pre-requisite and propagation delays.*

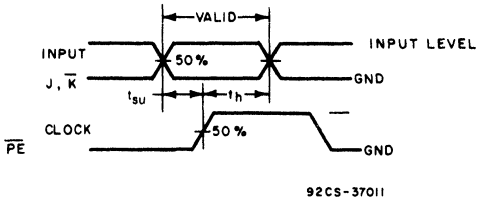
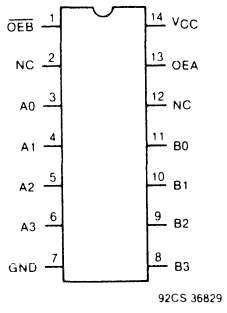



*Fig. 5 - J, $\overline{K}$ or Parallel Enable pre-requisite times.*

| | HC | HCT |
|---|---|---|
| Input Level | $V_{CC}$ | 3 V |
| $V_S$ | 50% | 1.3 V |

File Number **1488**

**Preliminary Data**




**TERMINAL ASSIGNMENT**

# Quad-Bus Transceiver with 3-State Outputs

**Type Features:**

- *Typical propagation delay (A⟶B) of 9 ns @ $V_{CC}$=5 V $C_L$=15 pF, $T_A$=25°C*
- *3-state outputs*
- *Buffered inputs*

**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT: −40 to +85°C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$=20%, $N_{IH}$=30% of $V_{CC}$; @ $V_{CC}$=5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$=0.8 V Max., $V_{IH}$=2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN}$ ≤ 1 μA @ $V_{OL}$, $V_{OH}$*

The RCA-CD54/74HC242, 243 and CD54/74HCT242, 243 silicon-gate CMOS 3-state bidirectional inverting and non-inverting buffers are intended for two-way asynchronous communication between data busses. They have high drive current outputs which enable high-speed operation when driving large bus capacitances. These circuits possess the low power dissipation associated with CMOS circuits, but speeds comparable to low power Schottky TTL circuits. They can also drive 15 LSTTL loads.

The CD54/74HC242 and CD54/74HCT242 are inverting buffers and the CD54/74HC243 and CD54/74HCT243 are non-inverting buffers.

The states of the output enables ($\overline{OEB}$, OEA) determine both the direction of flow (A to B, B to A), and the 3-state mode.

The CD54HC242, 243 and the CD54HCT242, 243 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC242, 243 and CD74HCT242, 243 are supplied in 14-lead dual-in-line plastic packages (E suffix).

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I$ < -0.5 V OR $V_I$ > $V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_o$ < -0.5 V OR $V_o$ > $V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR -0.5 V < $V_o$ < $V_{CC}$ + 0.5 V) ..... ±35 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±70 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = -55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

**RECOMMENDED OPERATING CONDITIONS:**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$=Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{in}$, $V_{out}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times $t_r$,$t_f$ | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC242/243/CD54HC242/243 | | | | | | | | | | CD74HCT242/243/CD54HCT242/243 | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC Series | | | 74HC Series | | 54HC Series | | TEST CONS. | | 74HCT/54HCT Series | | | 74HCT Series | | 54HCT Series | | | |
| | $V_{IN}$ V | | $V_{CC}$ V | +25°C Min | +25°C Typ | +25°C Max | -40/ +85°C Min | -40/ +85°C Max | -55/ +125°C Min | -55/ +125°C Max | $V_{IN}$ V | $V_{CC}$ V | +25°C Min | +25°C Typ | +25°C Max | -40/ +85°C Min | -40/ +85°C Max | -55/ +125°C Min | -55/ +125°C Max | | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | — | 4.5 | 2 | — | — | 2 | — | 2 | — | | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | 5.5 | | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | — | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | 5.5 | | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=-20μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | — | — | — | — | — | — | — | | |
| TTL Loads (Bus Driver) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) -6 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | | V |
| | | -7.8 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | — | — | — | — | — | — | — | | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20 μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | — | — | — | — | — | — | — | | |
| TTL Loads (Bus Driver) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) -6 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | | V |
| | | -7.8 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | — | — | — | — | — | — | — | | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 8 | — | 80 | — | 160 | $V_{CC}$ or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | | μA |
| 3-State Leakage Current | $V_{IL}$ or $V_{IH}$ | $V_O$=$V_{CC}$ or Gnd | 6 | — | — | ±0.5 | — | ±5.0 | — | ±10 | $V_{IL}$ or $V_{IH}$ | 5.5 | — | — | ±0.5 | — | ±5.0 | — | ±10 | | μA |

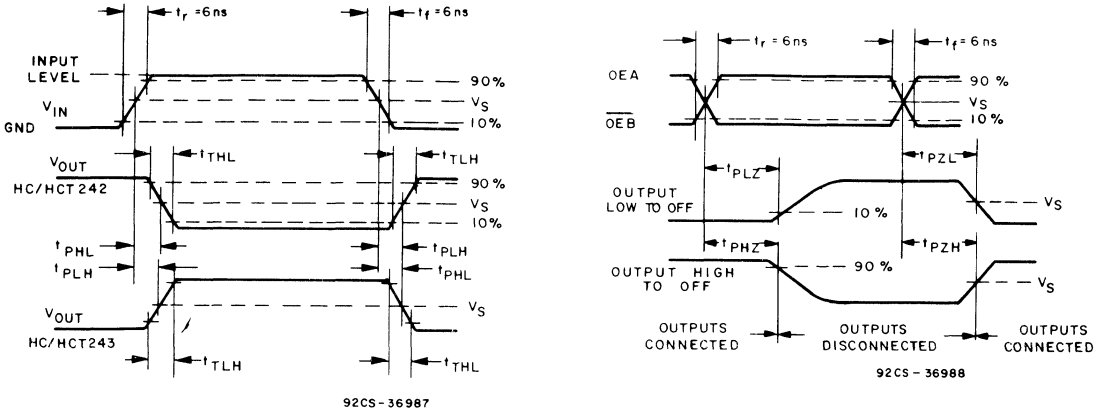
**SWITCHING CHARACTERISTICS ($V_{CC}$=5 V, $C_L$=15 pF, $T_A$=25° C, Input $t_r$,$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | 54/74HC/HCT | |
|---|---|---|---|
| | | Typical | Units |
| Propagation Delay Data to Output | $t_{PHL}$ $t_{PLH}$ | 9 | ns |
| Enable to High Z | | 14 | ns |
| Enable from High-Z | | 14 | ns |
| Power Dissipation Capacitance* | $C_{PD}$ | 33 | pF |
| Input Capacitance | $C_{IN}$ | 3.5 | pF |

*$C_{PD}$ is used to determine the dynamic power consumption, per flip-flop.
PD = $C_{PD}$ $Vcc^2$ fi + Σ ($C_L$ $Vcc^2$ f0 where:
fi=input frequency
fo=output frequency
$C_L$=output load capacitance
$V_{CC}$=supply voltage

**SWITCHING CHARACTERISTICS ($C_L$=50 pF, Input $t_r$,$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay Data to Outputs HC/HCT242 | $t_{PLH}$ $t_{PHL}$ | 2 | — | 125 | — | — | — | 155 | — | — | — | 190 | — | — | ns |
| | | 4.5 | — | 25 | — | — | — | 31 | — | — | — | 38 | — | — | |
| | | 6 | — | 21 | — | — | — | 26 | — | — | — | 32 | — | — | |
| Propagation Delay Data to Outputs for HC/HCT243 | $t_{PLH}$ $t_{PHL}$ | 2 | — | 100 | — | — | — | 125 | — | — | — | 150 | — | — | ns |
| | | 4.5 | — | 20 | — | — | — | 25 | — | — | — | 30 | — | — | |
| | | 6 | — | 17 | — | — | — | 21 | — | — | — | 26 | — | — | |
| Output High-Z to High Level | $t_{PZH}$ | 2 | — | 175 | — | — | — | 220 | — | — | — | 265 | — | — | ns |
| | | 4.5 | — | 35 | — | — | — | 44 | — | — | — | 53 | — | — | |
| | | 6 | — | 30 | — | — | — | 37 | — | — | — | 45 | — | — | |
| Output High-Z to Low Level | $t_{PZL}$ | 2 | — | 175 | — | — | — | 220 | — | — | — | 265 | — | — | ns |
| | | 4.5 | — | 35 | — | — | — | 44 | — | — | — | 53 | — | — | |
| | | 6 | — | 30 | — | — | — | 37 | — | — | — | 45 | — | — | |
| Output High Level to High-Z | $t_{PHZ}$ | 2 | — | 175 | — | — | — | 220 | — | — | — | 265 | — | — | ns |
| | | 4.5 | — | 35 | — | — | — | 44 | — | — | — | 53 | — | — | |
| | | 6 | — | 30 | — | — | — | 37 | — | — | — | 45 | — | — | |
| Output Low Level to High-Z | $t_{PLZ}$ | 2 | — | 175 | — | — | — | 220 | — | — | — | 265 | — | — | ns |
| | | 4.5 | — | 35 | — | — | — | 44 | — | — | — | 53 | — | — | |
| | | 6 | — | 30 | — | — | — | 37 | — | — | — | 45 | — | — | |
| Output Transition Time | $t_{TLH}$ $t_{THL}$ | 2 | — | 60 | — | — | — | 75 | — | — | — | 90 | — | — | ns |
| | | 4.5 | — | 12 | — | — | — | 15 | — | — | — | 18 | — | — | |
| | | 6 | — | 10 | — | — | — | 13 | — | — | — | 15 | — | — | |




| | 54/74HC | 54/74HCT |
|---|---|---|
| Input Level | $V_{CC}$ | 3 V |
| $V_S$ | 50% $V_{CC}$ | 1.3 V |

*Fig. 1 - Transition times and propagation delay times.*

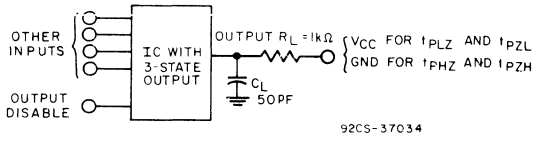



*Fig. 2 - Three-state propagation delay test circuit.*

**TRUTH TABLE**

| CONTROL INPUTS | | HC,HCT242 Series DATA PORT STATUS | | HC,HCT243 Series DATA PORT STATUS | |
|---|---|---|---|---|---|
| $\overline{OEB}$ | OEA | $A_n$ | $B_n$ | $A_n$ | $B_n$ |
| H | H | $\overline{O}$ | I | O | I |
| L | H | Z | Z | Z | Z |
| H | L | Z | Z | Z | Z |
| L | L | I | $\overline{O}$ | I | O |

H = High
L = Low
I = Input
O = Output
$\overline{O}$ = Inverting Output
Z = High Impedance

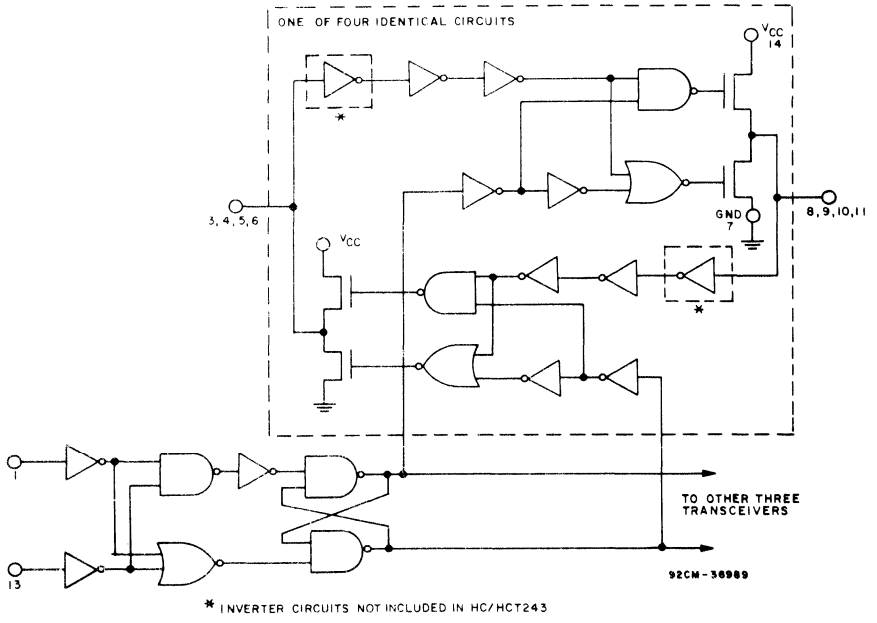



*Fig. 3 - Logic diagram for HC/HCT242, 243.*

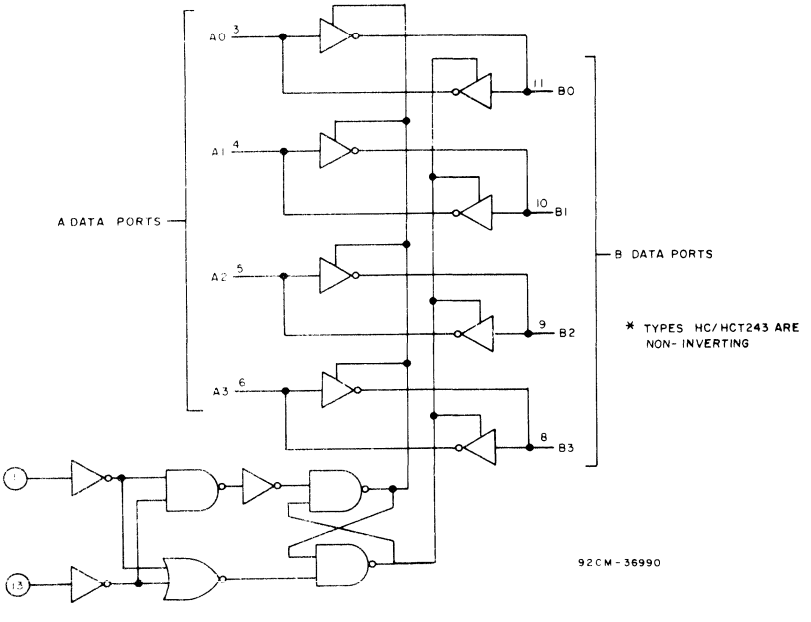
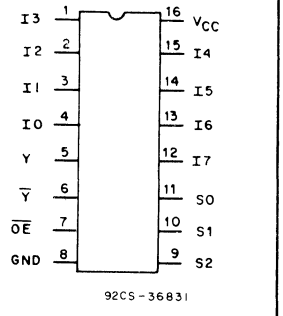



*Fig. 4 - Functional diagram for HC/HCT242, 243 *.*

**Preliminary Data**

File Number **1489**




**TERMINAL ASSIGNMENT**

# 8-Input Multiplexer; 3-State

**Type Features:**

- *Selects one of eight binary data inputs*
- *3-state output capability*
- *True and complement outputs*
- *Typical (data to output) propagation delay of 14 ns @ $V_{CC}$=5 V, $C_L$=15 pF, $T_A$=+25° C*

**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT: 40 to +85° C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$=20%, $N_{IH}$=30% of $V_{CC}$; @ $V_{CC}$=5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$=0.8 V Max., $V_{IH}$=2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN} \leq 1\ \mu A$ @ $V_{OL}$, $V_{OH}$*

The RCA-CD54/74HC251 and CD54/74HCT251 are 8-channel digital multiplexers with 3-state outputs, fabricated with high-speed silicon-gate CMOS technology. Together with the low power consumption of standard CMOS integrated circuits, they possess the ability to drive 10 LSTTL loads. The 3-state feature makes them ideally suited for interfacing with bus lines in a bus-oriented system.

This multiplexer features both true (Y) and complement ($\overline{Y}$) outputs as well as an output enable ($\overline{OE}$) input. The $\overline{OE}$ must be at a low logic level to enable this device. When the $\overline{OE}$ input is high, both outputs are in the high-impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and $\overline{Y}$ outputs. The CD54/74HCT251 logic family is speed, function, and pin-compatible with the standard 54LS/74LS251.

The CD54HC251 and CD54HCT251 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC251 and CD74HCT251 are supplied in 16-lead dual-in-line plastic packages (E suffix).

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR -0.5 V < $V_O$ < $V_{CC}$ + 0.5 V) ..... ±25 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±50 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = -55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

**RECOMMENDED OPERATING CONDITIONS:**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS MIN. | LIMITS MAX. | UNITS |
|---|---|---|---|
| Supply-Voltage Range (For $T_A$=Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{in}$, $V_{out}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times $t_r$,$t_f$ | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC251/CD54HC251 TEST CONDITIONS $V_{IN}$ V | $I_O$ (mA) | $V_{CC}$ V | 74HC/54HC Series +25°C Min | Typ | Max | 74HC Series -40/+85°C Min | Max | 54HC Series -55/+125°C Min | Max | CD74HCT251/CD54HCT251 TEST CONS. $V_{IN}$ V | $V_{CC}$ V | 74HCT/54HCT Series +25°C Min | Typ | Max | 74HCT Series -40/+85°C Min | Max | 54HCT Series -55/+125°C Min | Max | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | — | 4.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | 5.5 | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | — | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | 5.5 | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=-20μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | | | | | | | | |
| TTL Loads (Standard Outputs) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) -4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | -5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | | | | | | | | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20 μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | |
| TTL Loads (Standard Outputs) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) -4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V |
| | | -5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | | | | | | | | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 8 | — | 80 | — | 160 | $V_{CC}$ or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | μA |
| 3-State Leakage Current | $V_{IL}$ or $V_{IH}$ | $V_O$=$V_{CC}$ or Gnd | 6 | — | — | ±0.5 | — | ±5.0 | — | ±10 | $V_{IL}$ or $V_{IH}$ | 5.5 | — | — | ±0.5 | — | ±5.0 | — | ±10 | μA |

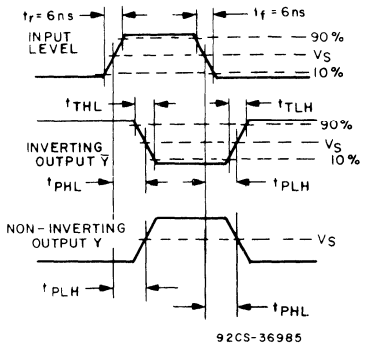
**SWITCHING CHARACTERISTICS ($V_{CC}$=5 V, $C_L$=15 pF, $T_A$=25° C, Input $t_r$,$t_f$=6 ns)**

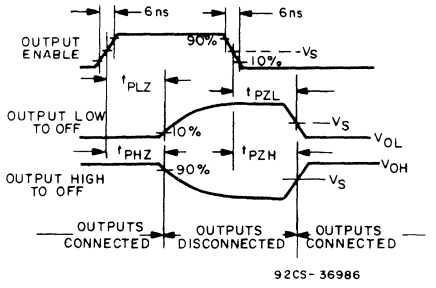
| CHARACTERISTIC | | SYMBOL | 54/74HC/HCT | |
|---|---|---|---|---|
| | | | Typical | Units |
| Propagation Delay | Select to Outputs | $t_{PHL}$ $t_{PLH}$ | 17 | ns |
| | Data to Outputs | | 14 | ns |
| | Enable to High-Z and Enable from High-Z | | 14 | ns |
| Power Dissipation Capacitance* | | $C_{PD}$ | 25 | pF |
| Input Capacitance | | $C_{IN}$ | 3.5 | pF |

*$C_{PD}$ is used to determine the dynamic power consumption, per flip-flop.
$PD = C_{PD} Vcc^2 fi + \Sigma\ C_L Vcc^2 fo$ where:
fi=input frequency
fo=output frequency
$C_L$=output load capacitance
$V_{CC}$=supply voltage

**SWITCHING CHARACTERISTICS ($C_L$=50 pF, Input $t_r$,$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay Select to Outputs | $t_{PLH}$ $t_{PHL}$ | 2 | — | 200 | — | — | — | 250 | — | — | — | 300 | — | — | ns |
| | | 4.5 | — | 40 | — | 40 | — | 50 | — | 50 | — | 60 | — | 60 | |
| | | 6 | — | 34 | — | — | — | 43 | — | — | — | 51 | — | — | |
| Propagation Delay Data to Outputs | $t_{PLH}$ $t_{PHL}$ | 2 | — | 175 | — | — | — | 220 | — | — | — | 265 | — | — | ns |
| | | 4.5 | — | 35 | — | 35 | — | 44 | — | 44 | — | 53 | — | 53 | |
| | | 6 | — | 30 | — | — | — | 37 | — | — | — | 45 | — | — | |
| Output High-Z to High Level | $t_{PZH}$ | 2 | — | 175 | — | — | — | 220 | — | — | — | 265 | — | — | ns |
| | | 4.5 | — | 35 | — | 35 | — | 44 | — | 44 | — | 53 | — | 53 | |
| | | 6 | — | 30 | — | — | — | 37 | — | — | — | 45 | — | — | |
| Output High-Z to Low Level | $t_{PZL}$ | 2 | — | 175 | — | — | — | 220 | — | — | — | 265 | — | — | ns |
| | | 4.5 | — | 35 | — | 35 | — | 44 | — | 44 | — | 53 | — | 53 | |
| | | 6 | — | 30 | — | — | — | 37 | — | — | — | 45 | — | — | |
| Output High Level to High-Z | $t_{PHZ}$ | 2 | — | 175 | — | — | — | 220 | — | — | — | 265 | — | — | ns |
| | | 4.5 | — | 35 | — | 35 | — | 44 | — | 44 | — | 53 | — | 53 | |
| | | 6 | — | 30 | — | — | — | 37 | — | — | — | 45 | — | — | |
| Output Low Level to High-Z | $t_{PLZ}$ | 2 | — | 175 | — | — | — | 220 | — | — | — | 265 | — | — | ns |
| | | 4.5 | — | 35 | — | 35 | — | 44 | — | 44 | — | 53 | — | 53 | |
| | | 6 | — | 30 | — | — | — | 37 | — | — | — | 45 | — | — | |
| Output Transition Time | $t_{TLH}$ $t_{THL}$ | 2 | — | 75 | — | — | — | 95 | — | — | — | 110 | — | — | ns |
| | | 4.5 | — | 15 | — | 15 | — | 19 | — | 19 | — | 22 | — | 22 | |
| | | 6 | — | 13 | — | — | — | 16 | — | — | — | 19 | — | — | |




| | 54/74HC | 54/74HCT |
|---|---|---|
| Input Level | $V_{CC}$ | 3 V |
| $V_S$ | 50% $V_{CC}$ | 1.3 V |

*Fig. 1 - Transition times and propagation delay times.*

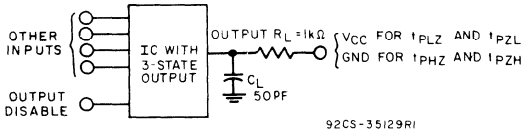



*Fig. 2 - Three-state propagation delay test circuit.*

**TRUTH TABLE**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| SELECT | | | OUTPUT | | |
| S2 | S1 | S0 | CONTROL $\overline{OE}$ | Y | $\overline{Y}$ |
| X | X | X | H | Z | Z |
| L | L | L | L | I0 | $\overline{I0}$ |
| L | L | H | L | I1 | $\overline{I1}$ |
| L | H | L | L | I2 | $\overline{I2}$ |
| L | H | H | L | I3 | $\overline{I3}$ |
| H | L | L | L | I4 | $\overline{I4}$ |
| H | L | H | L | I5 | $\overline{I5}$ |
| H | H | L | L | I6 | $\overline{I6}$ |
| H | H | H | L | I7 | $\overline{I7}$ |

H = high logic level
L = low logic level
X = irrelevant
Z = high impedance (off)
I0, I1 . . . I7 = the level of the respective input

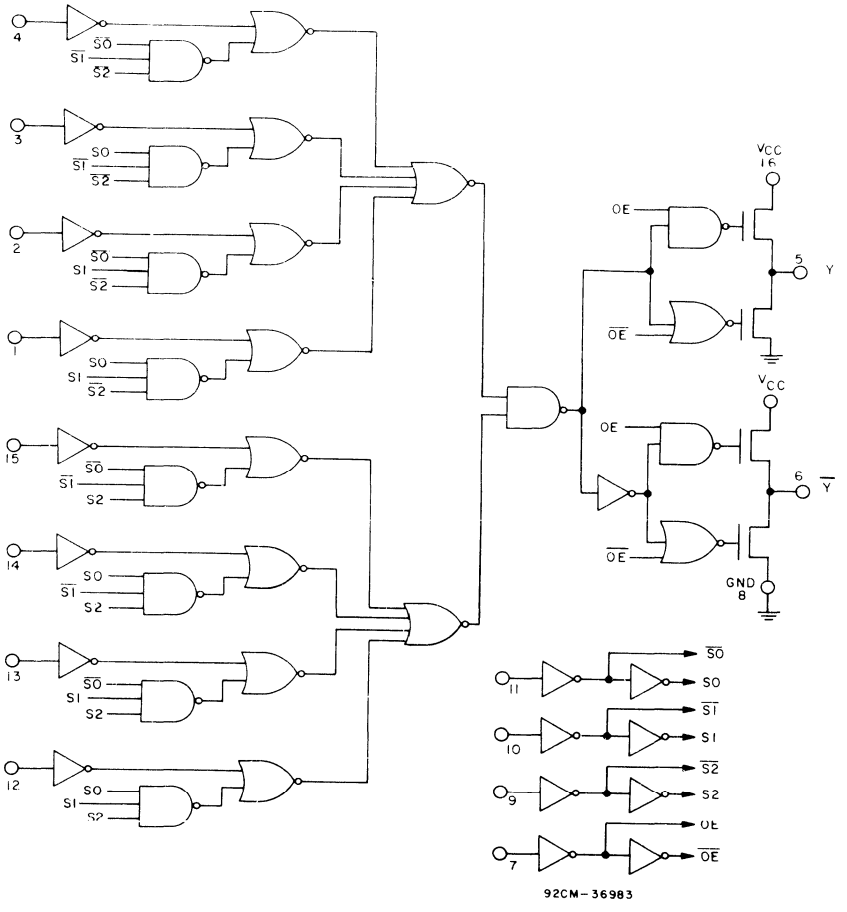



*Fig. 3 - Logic diagram for HC/HCT251.*

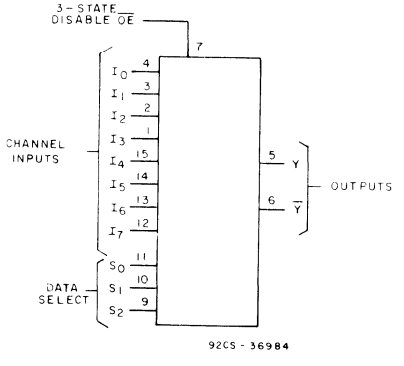
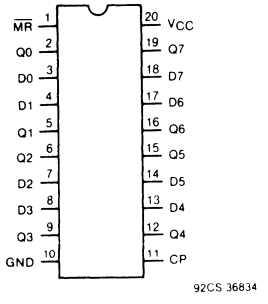



*Fig. 4 - Functional diagram for HC/HCT251.*

File Number **1479**

**Preliminary Data**




**TERMINAL ASSIGNMENT**

# Octal D Flip-Flop with Reset

**Type Features:**

- *Common Clock and Asynchronous Master Reset*
- *Positive edge triggering*
- *Buffered Inputs*
- *Typical $F_{max}$ = 50 MHz @ $V_{CC}$ = 5.0 V, $C_L$ = 15 pF, $T_A$ = 25° C*

**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*

The RCA CD54/74HC273 and the CD54/74HCT273 high speed Octal D-Type Flip-Flops with a direct clear input are manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits.

Information at the D input is transferred to the Q outputs on the positive-going edge of the clock pulse. All eight Flip-Flops are controlled by a common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock. All eight Q outputs are reset to a logic 0.

The CD54HC273 and CD54HCT273 are supplied in 20-lead hermetic dual-in-line ceramic packages (F-suffix) and the CD74HC273 and CD74HCT273 are supplied in 20-lead dual-in-line plastic packages (E-suffix).

- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$ = 20%, $N_{IH}$ = 30% of $V_{CC}$; @ $V_{CC}$ = 5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$ = 0.8 V Max., $V_{IH}$ = 2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN} \leq 1\ \mu A$ @ $V_{OL}$, $V_{OH}$*

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR -0.5 V < $V_O$ < $V_{CC}$ +0.5 V) ..... ±25 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±50 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = -55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

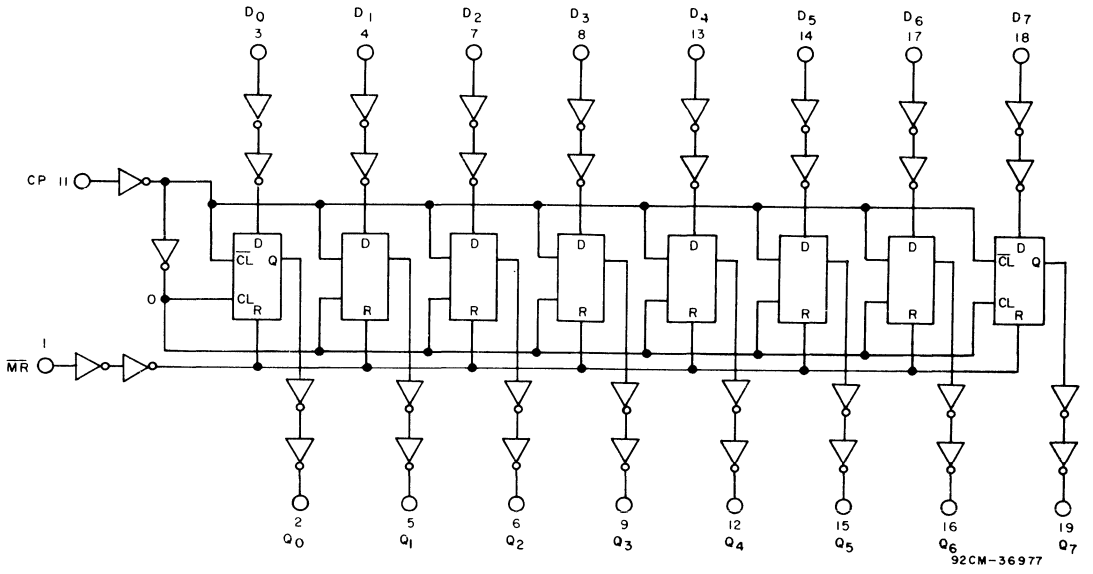



*Fig. 1 - Logic diagram.*

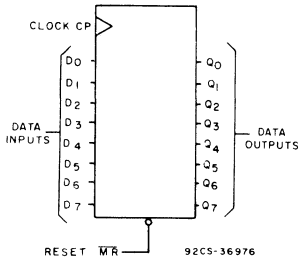



*Fig. 2 - Functional diagram.*

**TRUTH TABLE**
**(EACH FLIP-FLOP)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| **RESET ($\overline{MR}$)** | **CLOCK CP** | **DATA Dn** | **Q** |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | $Q_0$ |

H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
↑ = Transition from Low to High Level
$Q_0$ = The Level of Q Before the Indicated Steady-State Input Conditions were Established

**RECOMMENDED OPERATING CONDITIONS:**
**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply Voltage Range (For $T_A$ = Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{IN}$, $V_{OUT}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times, tr, tf | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC273/CD54HC273 | | | | | | | | | | CD74HCT273/CD54HCT273 | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC Series | | | 74HC Series | | 54HC Series | | TEST CONS. | | 74HCT/54HCT Series | | | 74HCT Series | | 54HCT Series | | |
| | $V_{IN}$ V | | $V_{CC}$ V | +25°C Min | +25°C Typ | +25°C Max | -40/+85°C Min | -40/+85°C Max | -55/+125°C Min | -55/+125°C Max | $V_{IN}$ V | $V_{CC}$ V | +25°C Min | +25°C Typ | +25°C Max | -40/+85°C Min | -40/+85°C Max | -55/+125°C Min | -55/+125°C Max | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | | 4.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | 5.5 | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | 5.5 | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=-20μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | | | | | | | | | |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | — | — | — | — | — | — | — | — | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) -4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | | | | | | | | | |
| | | | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | -5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | — | — | — | — | — | — | — | — | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | | | | | | | | | |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | — | — | — | — | — | — | — | — | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) 4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | $V_{IL}$ or $V_{IH}$ | | | | | | | | | |
| | | | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V |
| | | 5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | — | — | — | — | — | — | — | — | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 8 | — | 80 | — | 160 | $V_{CC}$ or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | μA |

**SWITCHING CHARACTERISTICS ($V_{CC}$ = 5 V, $T_A$ = 25° C, Input $t_r$ = $t_f$ = 6 ns)**

| CHARACTERISTIC | | 54/74HC/HCT TYPICAL | UNIT |
|---|---|---|---|
| Propagation Delay, ($C_L$ = 15 pF) Clock to Q | $t_{PLH}$ $t_{PHL}$ | 13 | ns |
| Maximum Clock Frequency ($C_L$ = 15 pF) | $f_{max}$ | 50 | MHz |
| Input Capacitance | $C_{in}$ | 3.5 | pF |
| Power Dissipation Capacitance* | $C_{PD}$ | 45 | pF |

*$C_{PD}$ is used to determine the dynamic power consumption, per flip-flop.

$P_D = C_{PD}V_{CC}^2f_i + \Sigma\ C_LV_{CC}^2f_o$ where $f_i$ = input frequency, $f_o$ = output frequency,

$C_L$ = output load capacitance, $V_{CC}$ = supply voltage

**PRE-REQUISITE FOR SWITCHING FUNCTION**

| CHARACTERISTIC | | TEST CONDITION | LIMITS | | | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | |
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | $V_{CC}$ V | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Minimum Clock Frequency Fig. 3 | $f_{max}$ | 2 | 6 | | — | | 5 | | — | | 4 | | — | | MHz |
| | | 4.5 | 30 | | 25 | | 25 | | 20 | | 20 | | 16 | | |
| | | 6 | 35 | | — | | 29 | | — | | 23 | | — | | |
| $\overline{MR}$ Pulse Width Fig. 4 | $t_w$ | 2 | 80 | | — | | 100 | | — | | 120 | | — | | ns |
| | | 4.5 | 16 | | 20 | | 20 | | 25 | | 29 | | 30 | | |
| | | 6 | 14 | | — | | 17 | | — | | 20 | | — | | |
| Clock Pulse Width Fig. 3 | $t_w$ | 2 | 80 | | — | | 100 | | — | | 120 | | — | | ns |
| | | 4.5 | 16 | | 20 | | 20 | | 25 | | 24 | | 30 | | |
| | | 6 | 14 | | — | | 17 | | — | | 20 | | — | | |
| Set-up Time DS0, DS7, I/on to Clock Fig. 5 | $t_{su}$ | 2 | 100 | | — | | 125 | | — | | 150 | | — | | ns |
| | | 4.5 | 20 | | 20 | | 25 | | 25 | | 30 | | 30 | | |
| | | 6 | 17 | | — | | 21 | | — | | 26 | | — | | |
| Hold Time DS0, DS7, I/on to Clock Fig. 5 | $t_H$ | 2 | | 3 | | — | | 3 | | — | | 3 | | — | ns |
| | | 4.5 | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | |
| | | 6 | | 3 | | — | | 3 | | — | | 3 | | — | |
| Removal Time $\overline{MR}$ to Clock | $t_{REM}$ | 2 | | 5 | | — | | 5 | | — | | 5 | | — | ns |
| | | 4.5 | | 5 | | 5 | | 5 | | 5 | | 5 | | 5 | |
| | | 6 | | 5 | | — | | 5 | | — | | 5 | | — | |

**SWITCHING CHARACTERISTICS ($C_L$ = 50 pF, Input $t_r$ = $t_f$ = 6 ns)**

| CHARACTERISTIC | | TEST CONDITION Vcc V | LIMITS | | | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | |
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay | $t_{PLH}$ | 2 | | 150 | | — | | 190 | | — | | 225 | | — | |
| Clock to Output | $t_{PHL}$ | 4.5 | | 30 | | 35 | | 38 | | 44 | | 45 | | 53 | ns |
| Fig. 3 | | 6 | | 26 | | — | | 33 | | — | | 38 | | — | |
| Propagation Delay | | 2 | | 150 | | — | | 190 | | — | | 225 | | — | |
| $\overline{MR}$ to Output | $t_{PHL}$ | 4.5 | | 30 | | 35 | | 38 | | 44 | | 45 | | 53 | ns |
| Fig. 4 | | 6 | | 26 | | — | | 33 | | — | | 38 | | — | |
| Output Transition | $t_{TLH}$ | 2 | | 75 | | — | | 95 | | — | | 110 | | — | |
| Time | $t_{THL}$ | 4.5 | | 15 | | 15 | | 19 | | 19 | | 22 | | 22 | ns |
| Fig. 6 | | 6 | | 13 | | — | | 16 | | — | | 19 | | — | |

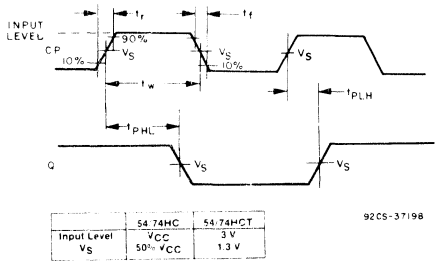



*Fig. 3 - Clock to output delays a clock pulse width.*

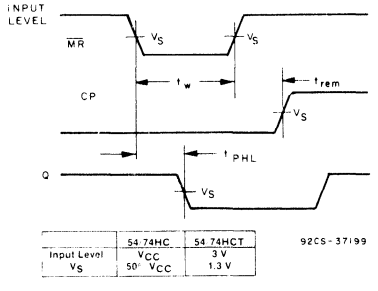



*Fig. 4 - Master reset pulse width. Master reset to output delay and master reset to clock recovery time.*

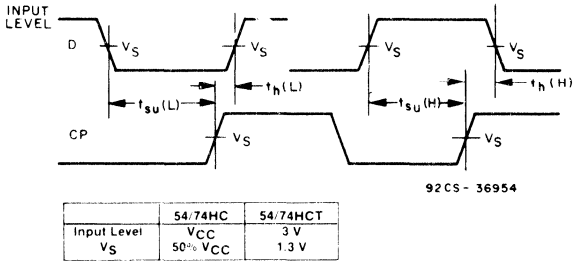



*Fig. 5 - Data set-up and hold times.*

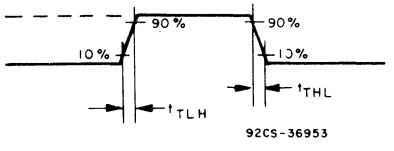
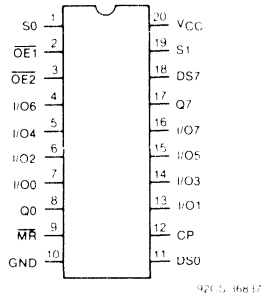



*Fig. 6 - Transition times and propagation delay times, combination logic.*

**Preliminary Data**

File Number **1485**




**TERMINAL ASSIGNMENT**

# 8-Bit Universal Shift Register; 3-State

**Type Features:**

- *Four Operation Modes: Shift Left, Shift Right, Load and Store*
- *Can be cascaded for N-bit word lengths*
- *$I/O_0$-$I/O_7$ bus drive capability and 3-state for bus oriented applications*
- *Buffered inputs*
- *Typical $f_{MAX}$=50 MHz @ $V_{CC}$=5 V, $C_L$=15 pF*

**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT/HCU: −40 to +85° C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$=20%, $N_{IH}$=30% of $V_{CC}$; @ $V_{CC}$=5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$=0.8 V Max., $V_{IH}$=2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN} \leq 1\ \mu A$ @ $V_{OL}$, $V_{OH}$*

The RCA-CD54/74HC299 and CD54/74HCT299 are 8-bit shift/storage registers with 3-state bus interface capability. The register has four synchronous-operating modes controlled by the two select inputs as shown in the mode select (S0, S1) table. The mode select, the serial data (DS0, DS7) and the parallel data ($I/O_0$-$I/O_7$) respond only to the low-to-high transition of the clock (CP) pulse. S0, S1 and data inputs must be one set-up time prior to the clock positive transition.

The Master Reset ($\overline{MR}$) is an asynchronous active low input. When $\overline{MR}$ output is low, the register is cleared regardless of the status of all other inputs. The register can be expanded by cascading same units by tying the serial output (Q0) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DS0) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DS0 of the first stage.

The 3-state input/output I(/O) port has three modes of operation:

1. Both output enable ($\overline{OE1}$ and $\overline{OE2}$) inputs are low and S0 or S1 or both are low, the data in the register is presented at the eight outputs.
2. When both S0 and S1 are high, I/O terminals are in the high impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of $\overline{OE1}$ and $\overline{OE2}$.
3. Either one of the two output enable inputs being high will force I/O terminals to be in the off-state. It is noted that each I/O terminal is a 3-state output and an CMOS buffer input.

The CD54HC299 and CD54HCT299 are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC299 and CD74HCT299 are supplied in 20-lead dual-in-line plastic packages (E suffix).

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR $-0.5 V < V_o < V_{CC} + 0.5$ V) ..... ±35 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±70 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = -55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

**RECOMMENDED OPERATING CONDITIONS:**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$=Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{in}$, $V_{out}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times $t_r$,$t_f$ | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**MODE SELECT-FUNCTION TABLE**

**REGISTER OPERATING MODES** =

| FUNCTION | INPUTS | | | | | | | REGISTER OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | CP | S0 | S1 | $DS_0$ | $DS_7$ | $I/O_n$ | Q0 | Q1 | --- | Q6 | Q7 |
| **Reset (Clear)** | L | X | X | X | X | X | X | L | L | --- | L | L |
| Shift Right | H | ↑ | h | l | l | X | X | L | $q_0$ | --- | $q_5$ | $q_6$ |
| | H | ↑ | h | l | h | X | X | H | $q_0$ | --- | $q_5$ | Q6 |
| Shift Left | H | ↑ | l | h | X | l | X | $q_1$ | q2 | --- | $q_7$ | L |
| | H | ↑ | l | h | X | h | X | $q_1$ | $q_2$ | --- | $q_7$ | H |
| Hold (do nothing) | H | ↑ | l | l | X | X | X | $q_0$ | $q_1$ | --- | $q_6$ | $q_7$ |
| Parallel Load | H | ↑ | h | h | X | X | l | L | L | --- | L | L |
| | H | ↑ | h | h | X | X | h | H | H | --- | H | H |

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CD74HC299/CD54HC299 | | | | | | | | | | CD74HCT299/CD54HCT299 | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC Series | | | 74HC Series | | 54HC Series | | TEST CONS. | | 74HCT/54HCT Series | | | 74HCT Series | | 54HCT Series | |
| | $V_{IN}$ V | | $V_{CC}$ V | +25°C | | | -40/ +85°C | | -55/ +125°C | | $V_{IN}$ V | $V_{CC}$ V | +25°C | | | -40/ +85°C | | -55/ +125°C | |
| | | | | Min | Typ | Max | Min | Max | Min | Max | | | Min | Typ | Max | Min | Max | Min | Max | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | — | 4.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | 5.5 | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | — | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | 5.5 | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=-20μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | — | — | — | — | — | — | — | |
| TTL Loads | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA)* $Q_N$ -4 -5.2 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | $\overline{Q}_N$ -6 -7.8 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | — | — | — | — | — | — | — | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20 μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | — | — | — | — | — | — | — | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | — | — | — | — | — | — | — | |
| TTL Loads | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA)* $Q_N$ -4 -5.2 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V |
| | | $\overline{Q}_N$ -6 -7.8 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | — | — | — | — | — | — | — | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 8 | — | 80 | — | 160 | $V_{CC}$ or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | μA |
| 3-State Leakage Current | $V_{IL}$ or $V_{IH}$ | $V_O$=$V_{CC}$ or Gnd | 6 | — | — | ±0.5 | — | ±5.0 | — | ±10 | $V_{IL}$ or $V_{IH}$ | 5.5 | — | — | ±0.5 | — | ±5.0 | — | ±10 | μA |

*$Q_N$, N=0, 7.
$I/O_N$, N=0, to 7.

## MODE-SELECT FUNCTION TABLE

### 3-STATE I/O PORT OPERATING MODE =

| FUNCTION | INPUTS | | | | | INPUTS/OUTPUTS |
|---|---|---|---|---|---|---|
| | $\overline{OE}_1$ | $\overline{OE}_2$ | S0 | S1 | $Q_n$ (Register) | $I/Q_0$ - - -$I/Q_7$ |
| Read Register | L | L | L | X | L | L |
| | L | L | L | X | H | H |
| | L | L | X | L | L | L |
| | L | L | X | L | H | H |
| Load Register | X | X | H | H | $Q_n = I/Q_n$ | $I/Q_n$ = Inputs |
| Disable I/O | H | X | X | X | X | (Z) |
| | X | H | X | X | X | (Z) |

Notes:
H=Input voltage high level.
h=Input voltage high one set-up time prior clock transition.
L=Input voltage low level.
l=Input voltage low one set-up time prior clock transition.
$q_n$=Lower case letter indicates the state of the referenced output one set-up time prior clock transition.
X=Voltage level on logic status don't care.
Z=Output in high impedance state.
↑=Low-to-high clock transition.

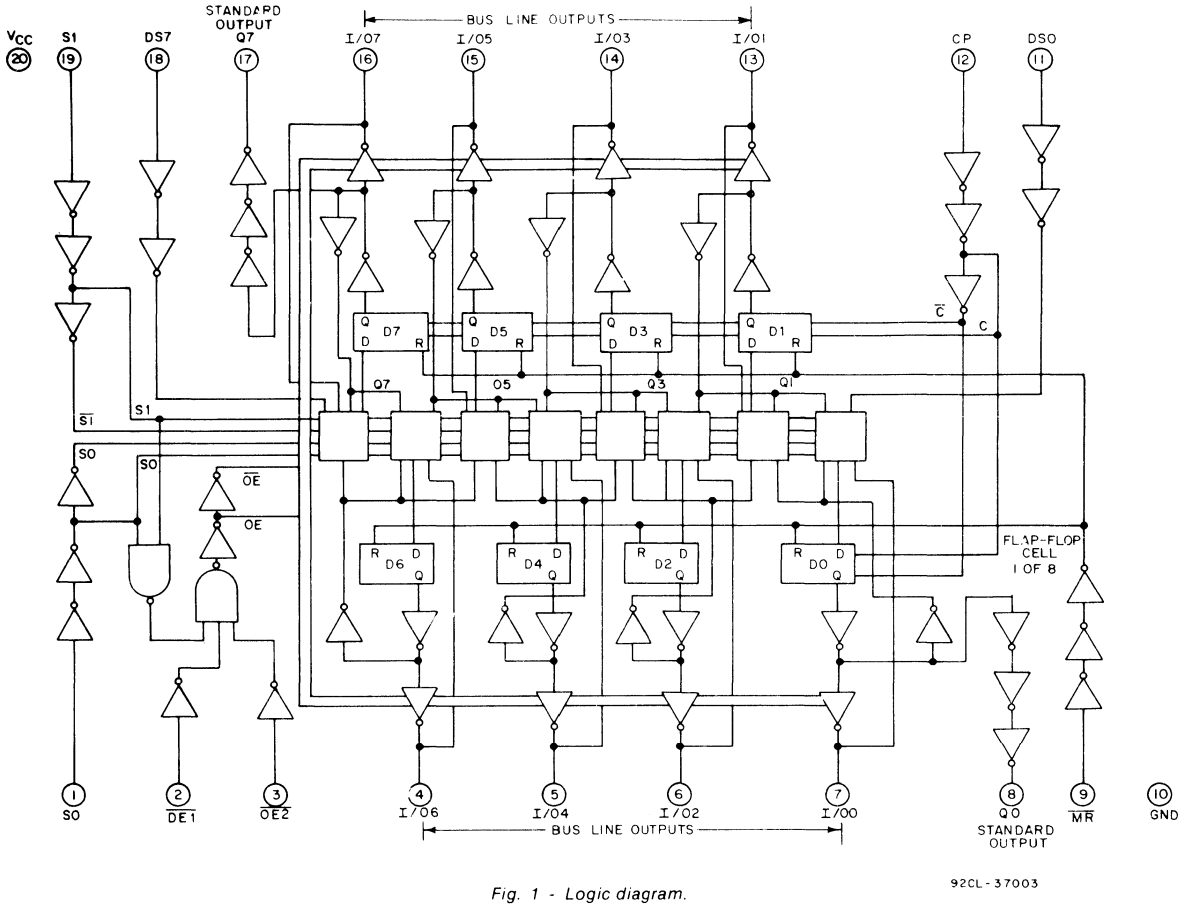



*Fig. 1 - Logic diagram.*

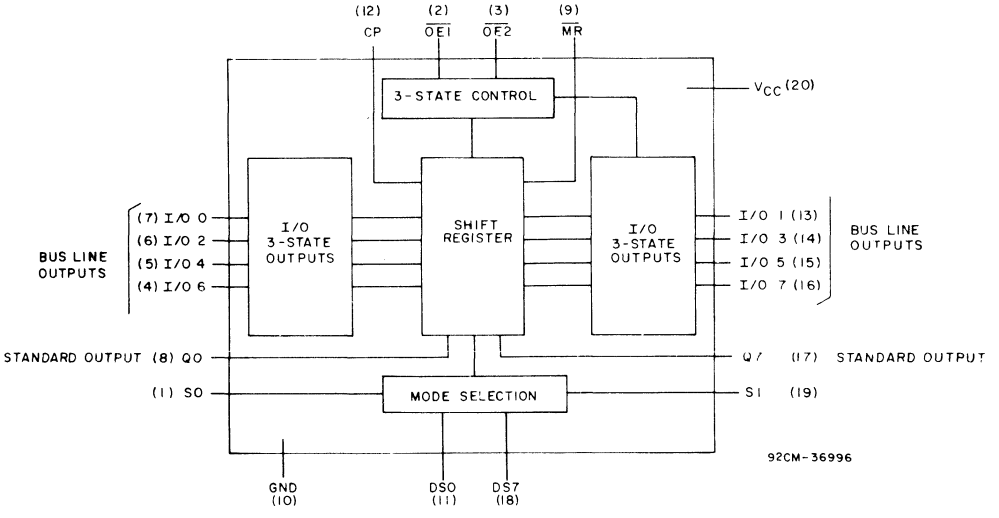



*Fig. 2 - Function diagram.*

**Pre-requisite for Switching**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Maximum Clock Frequency | $f_{MAX}$ | 2 | 6 | — | — | — | 5 | — | — | — | 4 | — | — | — | MHz |
| | | 4.5 | 30 | — | 25 | — | 25 | — | 20 | — | 20 | — | 16 | — | |
| | | 6 | 35 | — | — | — | 29 | — | — | — | 23 | — | — | — | |
| $\overline{MR}$ Pulse Width (Figure 4) | $t_W$ | 2 | 80 | — | — | — | 100 | — | — | — | 120 | — | — | — | ns |
| | | 4.5 | 16 | — | 20 | — | 20 | — | 25 | — | 24 | — | 30 | — | |
| | | 6 | 14 | — | — | — | 17 | — | — | — | 20 | — | — | — | |
| Clock Pulse Width (Figure 3) | $t_W$ | 2 | 80 | — | — | — | 100 | — | — | — | 120 | — | — | — | ns |
| | | 4.5 | 16 | — | 20 | — | 20 | — | 25 | — | 24 | — | 30 | — | |
| | | 6 | 14 | — | — | — | 17 | — | — | — | 20 | — | — | — | |
| Set-up Time DS0, DS7, $I/O_n$ to Clock S0, S1 (Figure 7) | $t_{SU}$ | 2 | 100 | — | — | — | 125 | — | — | — | 150 | — | — | — | ns |
| | | 4.5 | 20 | — | 20 | — | 25 | — | 25 | — | 30 | — | 30 | — | |
| | | 6 | 17 | — | — | — | 21 | — | — | — | 26 | — | — | — | |
| Hold Time DS0, DS7, $I/O_n$ to Clock S0, S1 (Figure 7) | $t_h$ | 2 | 0 | — | — | — | 0 | — | — | — | 0 | — | — | — | ns |
| | | 4.5 | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | |
| | | 6 | 0 | — | — | — | 0 | — | — | — | 0 | — | — | — | |
| Removal Time $\overline{MR}$ to Clock (Figure 4) | $t_{rem}$ | 2 | 80 | — | — | — | 100 | — | — | — | 120 | — | — | — | ns |
| | | 4.5 | 16 | — | 16 | — | 20 | — | 20 | — | 24 | — | 24 | — | |
| | | 6 | 14 | — | — | — | 17 | — | — | — | 20 | — | — | — | |

**SWITCHING CHARACTERISTICS ($C_L$=50 pF, Input $t_r$,$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay Clock to I/O Output (Figure 3) | $t_{PLH}$ | 2 | — | 150 | — | — | — | 190 | — | — | — | 225 | — | — | ns |
| | $t_{PHL}$ | 4.5 | — | 30 | — | 35 | — | 38 | — | 44 | — | 45 | — | 53 | |
| | | 6 | — | 26 | — | — | — | 33 | — | — | — | 38 | — | — | |
| Propagation Delay Clock to Q0 and Q7 (Figure 3) | $t_{PLH}$ | 2 | — | 150 | — | — | — | 190 | — | — | — | 225 | — | — | ns |
| | $t_{PHL}$ | 4.5 | — | 30 | — | 35 | — | 38 | — | 44 | — | 45 | — | 53 | |
| | | 6 | — | 26 | — | — | — | 33 | — | — | — | 38 | — | — | |
| Propagation Delay $\overline{MR}$ to Output (Figure 4) | $t_{PHL}$ | 2 | — | 150 | — | — | — | 190 | — | — | — | 225 | — | — | ns |
| | | 4.5 | — | 30 | — | 35 | — | 38 | — | 44 | — | 45 | — | 53 | |
| | | 6 | — | 26 | — | — | — | 33 | — | — | — | 38 | — | — | |
| Output High-Z to Low Level (Figure 6) | $t_{PZH}$ | 2 | — | 150 | — | — | — | 190 | — | — | — | 225 | — | — | ns |
| | | 4.5 | — | 30 | — | 30 | — | 38 | — | 38 | — | 45 | — | 45 | |
| | | 6 | — | 26 | — | — | — | 33 | — | — | — | 38 | — | — | |
| Output High Level to High-Z (Figure 5) | $t_{PHZ}$ | 2 | — | 150 | — | — | — | 190 | — | — | — | 225 | — | — | ns |
| | | 4.5 | — | 30 | — | 30 | — | 38 | — | 38 | — | 45 | — | 45 | |
| | | 6 | — | 26 | — | — | — | 33 | — | — | — | 38 | — | — | |
| Output Low Level to High-Z (Figure 6) | $t_{PLZ}$ | 2 | — | 150 | — | — | — | 190 | — | — | — | 225 | — | — | ns |
| | $t_{PZL}$ | 4.5 | — | 30 | — | 30 | — | 38 | — | 38 | — | 45 | — | 45 | |
| | | 6 | — | 26 | — | — | — | 33 | — | — | — | 38 | — | — | |
| Output Transition Time Q0, Q7 (Figure 8) | $t_{TLH}$ | 2 | — | 75 | — | — | — | 95 | — | — | — | 110 | — | — | ns |
| | $t_{THL}$ | 4.5 | — | 15 | — | 15 | — | 19 | — | 19 | — | 22 | — | 22 | |
| | | 6 | — | 13 | — | — | — | 16 | — | — | — | 19 | — | — | |
| Output Transition Time $I/O_0$ to $I/O_7$ (Figure 8) | $t_{TLH}$ | 2 | — | 60 | — | — | — | 75 | — | — | — | 90 | — | — | ns |
| | $t_{THL}$ | 4.5 | — | 12 | — | 12 | — | 15 | — | 15 | — | 18 | — | 18 | |
| | | 6 | — | 10 | — | — | — | 13 | — | — | — | 15 | — | — | |

**SWITCHING CHARACTERISTICS ($V_{CC}$=5 V, $T_A$=25° C, Input $t_r$,$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | 54/74HC/HCT | |
|---|---|---|---|
| | | Typical | Units |
| Propagation Delay Clock to I/O Outputs (Figure 3) $C_L$=15 pF | $t_{PLH}$ $t_{PHL}$ | 13 | ns |
| Propagation Delay Clock Q0 to Q7 (Figure 3) | $t_{PLH}$ $t_{PHL}$ | 13 | ns |
| Propagation Delay $\overline{MR}$ to Outputs $C_L$ = 15 pF (Figure 4) | $t_{PHL}$ | 12 | ns |
| Output High-Z to High Level $C_L$=15 pF (Figure 5) | $t_{PZH}$ | 12 | ns |
| Output High-Z to Low Level $C_L$=15 pF (Figure 6) | $t_{PZL}$ | 12 | ns |
| Output High Level to High-Z $C_L$=15 pF (Figure 5) | $t_{PHZ}$ | 12 | ns |
| Output Low Level to High-Z $C_L$=15 pF (Figure 6) | $t_{PLZ}$ | 12 | ns |
| Input Capacitance | $C_{in}$ | 3.5 | pF |
| Power Dissipation Capacitance* | $C_{PD}$ | 10 | pF |

*$C_{PD}$ is used to determine the dynamic power consumption, per register.

$PD = C_{PD} Vcc^2 fi + \Sigma C_L Vcc^2 fo$ where

fi = input frequency

fo = output frequency

$C_L$ = output load capacitance

Vcc = supply voltage.

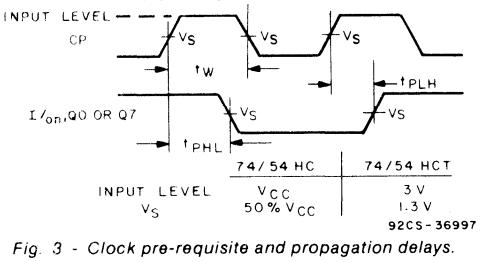



*Fig. 3 - Clock pre-requisite and propagation delays.*

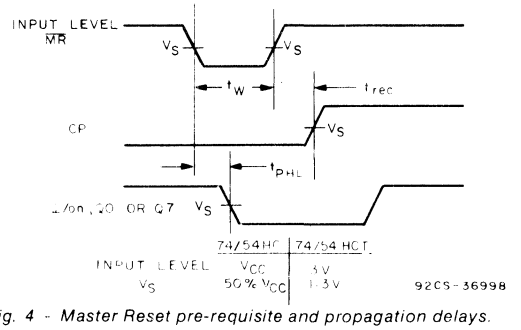



*Fig. 4 - Master Reset pre-requisite and propagation delays.*

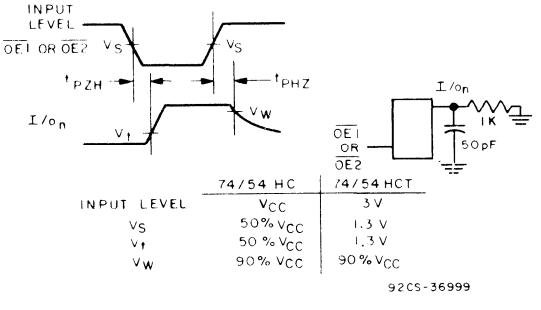



*Fig. 5 - Tri-state propagation delays.*

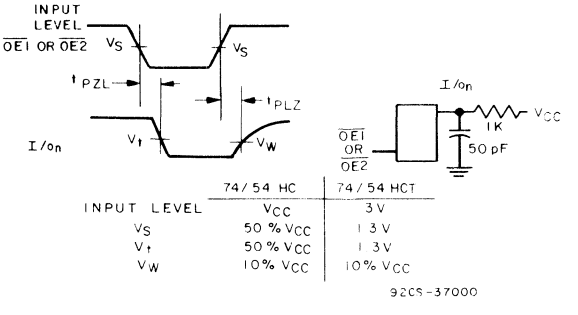



*Fig. 6 - Tri-state propagation delays.*

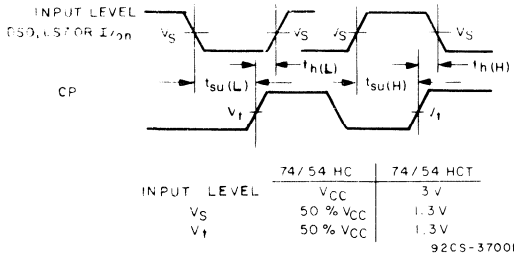



*Fig. 7 - Data pre-requisite times.*

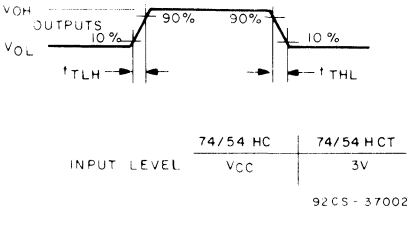
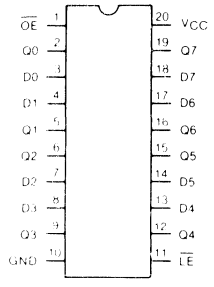



*Fig. 8 - Output transition times.*

**Preliminary Data**

File Number **1502**




**TERMINAL ASSIGNMENT**

# Octal Transparent Latch, 3-State Output

**Type Features:**

- *Common latch enable control*
- *Common 3-state output enable control*
- *Buffered inputs*
- *3-State outputs*
- *Bus line driving capacity*
- *Typical propagation delay = 14 ns @ VCC = 5.0 V, CL = 15 pF, TA = 25° C (Data to Output)*

**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT/HCU: -40 to +85° C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: NIL = 20%, NIH = 30% of VCC; @ VCC = 5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *VIL = 0.8 V Max., VIH = 2 V Min.*
  *CMOS Input Compatibility*
  *IIN ≤ 1 μA @ VOL, VOH*

The RCA CD54/74HC373 and CD54/74HCT373 are high speed Octal Transparent Latch manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL. The CD54/74HCT373 is functionally as well as pin compatible with the standard 54/74LS373.

The outputs are transparent to the inputs when the latch enable ($\overline{LE}$) is high. When the latch enable ($\overline{LE}$) goes low the data is latched. The output enable ($\overline{OE}$) controls the 3-state outputs. When the output enable ($\overline{OE}$) is high the outputs will be in the high impedance state. The latch operation is independent to the state of the output enable.

The CD54HC373 and CD54HCT373 are supplied in 20-lead hermetic dual-in-line ceramic packages (F Suffix). The CD74HC373 and CD74HCT373 are supplied in 20-lead dual-in-line plastic packages (E Suffix).

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (VCC):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, IIK (FOR VI < -0.5 V OR VI > VCC +0.5 V ..... ±20 mA
DC OUTPUT CURRENT, IOK (FOR VO < -0.5 V OR VO > VCC +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (IO) (FOR -0.5 V < VO < VCC +0.5 V) ..... ±35 mA
DC VCC OR GROUND CURRENT, PER PIN (ICC): ..... ±70 mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For TA = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For TA = -55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For TA = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE F ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE (Tstg) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

**RECOMMENDED OPERATING CONDITIONS:**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply Voltage Range (For $T_A$ = Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{IN}$, $V_{OUT}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times, tr, tf | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC373/CD54HC373 | | | | | | | | | | CD74HCT373/CD54HCT373 | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC Series | | | 74HC Series | | 54HC Series | | TEST COND. | | 74HCT/54HCT Series | | | 74HCT Series | | 54HCT Series | | | |
| | $V_{IN}$ V | | $V_{CC}$ V | +25°C Min | +25°C Typ | +25°C Max | -40/+85°C Min | -40/+85°C Max | -55/+125°C Min | -55/+125°C Max | $V_{IN}$ V | $V_{CC}$ V | +25°C Min | +25°C Typ | +25°C Max | -40/+85°C Min | -40/+85°C Max | -55/+125°C Min | -55/+125°C Max | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | | 4.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | 5.5 | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | 5.5 | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=-20μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | — | — | — | — | — | — | — | |
| TTL Loads (Bus Drive Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) -6.0 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | -7.8 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | — | — | — | — | — | — | — | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | — | — | — | — | — | — | — | |
| TTL Loads (Bus Drive Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) 6.0 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V |
| | | 7.8 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | — | — | — | — | — | — | — | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or $V_{SS}$ | $I_{OUT}$=0 | 6 | — | — | 8 | — | 80 | — | 160 | $V_{CC}$ or $V_{SS}$ | 5.5 | — | — | 8 | — | 80 | — | 160 | μA |
| 3-State Leakage Current $I_{OZ}$ | $V_{IL}$ or $V_{IH}$ | $V_O$=$V_{CC}$ or Gnd | 6 | — | — | ±0.5 | — | ±5.0 | — | ±10 | $V_{IL}$ or $V_{IH}$ | 5.5 | — | — | ±0.5 | — | ±5.0 | — | ±10 | μA |

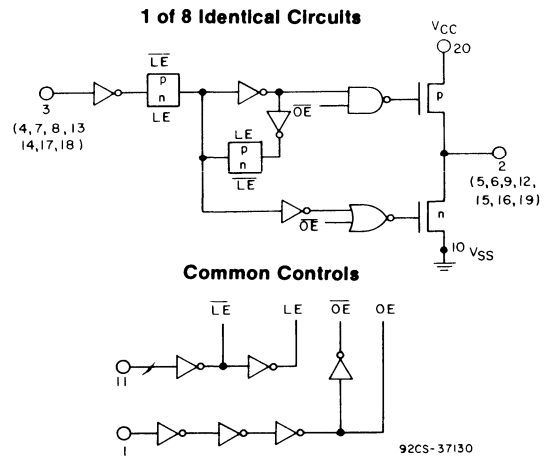



*Fig. 1 - Logic diagram.*

**TRUTH TABLE**

| Output Enable | Latch Enable | Data | Output |
|---|---|---|---|
| L | H | H | H |
| L | H | L | L |
| L | L | l | L |
| L | L | h | H |
| H | X | X | Z |

Note:
L = Low voltage level
H = High voltage level
l = Low voltage level one set-up time prior to the high to low latch enable transistion
h = High voltage level one set-up time prior to the high to low latch enable transistion
X = Don't care
Z = High impedance state

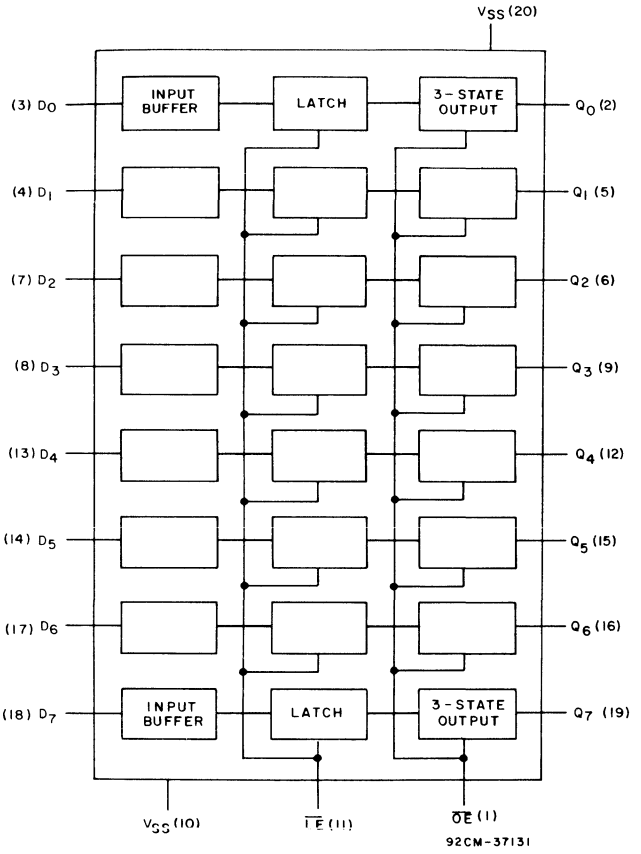



*Fig. 2 - Functional diagram.*

**SWITCHING CHARACTERISTICS ($V_{CC}$ = 5 V, $T_A$ = 25°C, Input $t_r$ = $t_f$ = 6 ns, $C_L$ = 15 pF)**

| CHARACTERISTIC | | 54/74HC/HCT TYPICAL | UNIT |
|---|---|---|---|
| Propagation Delay Data to QN Output (Fig. 3) | $t_{PLH}$ $t_{PHL}$ | 14 | ns |
| Propagation Delay $\overline{LE}$ to QN Output (Fig. 4) | $t_{PLH}$ $t_{PHL}$ | 14 | ns |
| Output High Z to High Level, (Fig. 6) | $t_{PZH}$ | 14 | ns |
| Output High Z to Low Level, (Fig. 7) | $t_{PZL}$ | 14 | ns |
| Output High Level to High Z, (Fig. 6) | $t_{PHZ}$ | 14 | ns |
| Output Low Level to High Z, (Fig. 7) | $t_{PLZ}$ | 14 | ns |
| Input Capacitance | $C_{in}$ | 3.5 | pF |
| Power Dissipation Capacitance | $C_{PD}$* | 50 | pF |

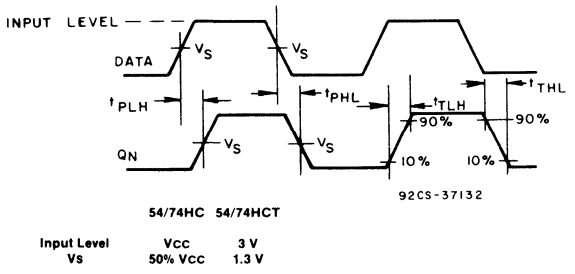
*$C_{PD}$ determines the no-load dynamic power consumption per latch. It is obtained by the following relationship;
$P_D$ (total power per latch) = $C_{PD}V_{CC}^2f_i + \Sigma\ C_LV_{CC}^2f_o$ where $f_i$ = input frequency, $f_o$ = output frequency,
$C_L$ = output load capacitance, $V_{CC}$ = supply voltage

**PRE-REQUISITE FOR SWITCHING FUNCTION**

| CHARACTERISTIC | | TEST CONDITION Vcc V | LIMITS 25°C HC Min. | HC Max. | HCT Min. | HCT Max. | -40°C to +85°C 74HC Min. | 74HC Max. | 74HCT Min. | 74HCT Max. | -55°C to +125°C 54HC Min. | 54HC Max. | 54HCT Min. | 54HCT Max. | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{LE}$ Pulse Width (Fig. 4) | $t_w$ | 2 | 80 | | — | | 100 | | — | | 120 | | — | | ns |
| | | 4.5 | 16 | | 20 | | 20 | | 25 | | 24 | | 30 | | |
| | | 6 | 14 | | — | | 17 | | — | | 20 | | — | | |
| Set-up Time Data to $\overline{LE}$ (Fig. 5) | $t_{su}$ | 2 | 100 | | — | | 125 | | — | | 150 | | — | | ns |
| | | 4.5 | 20 | | 20 | | 25 | | 25 | | 30 | | 30 | | |
| | | 6 | 17 | | — | | 21 | | — | | 26 | | — | | |
| Hold Time Data to $\overline{LE}$ (Fig. 5) | $t_H$ | 2 | 5 | | — | | 5 | | — | | 5 | | — | | ns |
| | | 4.5 | 5 | | 10 | | 5 | | 13 | | 5 | | 15 | | |
| | | 6 | 5 | | — | | 5 | | — | | 5 | | — | | |

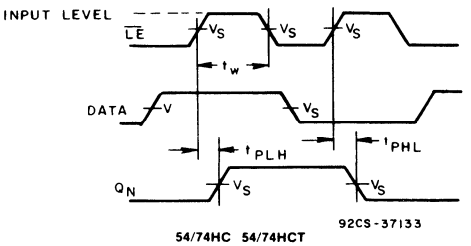
**SWITCHING CHARACTERISTICS (Input $t_r$, $t_f$ = 6 ns, $C_L$ = 50 pF)**

| CHARACTERISTIC | | TEST CONDITION Vcc V | LIMITS 25°C HC Min. | HC Max. | HCT Min. | HCT Max. | -40°C to +85°C 74HC Min. | 74HC Max. | 74HCT Min. | 74HCT Max. | -55°C to +125°C 54HC Min. | 54HC Max. | 54HCT Min. | 54HCT Max. | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Propagation Delay Data to QN Output N = 0 to 7, (Fig. 2) | $t_{PLH}$ | 2 | | 175 | | — | | 220 | | — | | 265 | | — | ns |
| | $t_{PHL}$ | 4.5 | | 35 | | 35 | | 44 | | 44 | | 53 | | 53 | |
| | | 6 | | 30 | | — | | 37 | | — | | 45 | | — | |
| Propagation Delay $\overline{LE}$ to QN Output N = 0 to 7, (Fig. 4) | $t_{PLH}$ | 2 | | 175 | | — | | 220 | | — | | 265 | | — | ns |
| | $t_{PHL}$ | 4.5 | | 35 | | 35 | | 44 | | 44 | | 53 | | 53 | |
| | | 6 | | 30 | | — | | 37 | | — | | 45 | | — | |
| Output High Z to High Level (Fig. 6) | $t_{PZH}$ | 2 | | 175 | | — | | 220 | | — | | 265 | | — | ns |
| | | 4.5 | | 35 | | 35 | | 44 | | 44 | | 53 | | 53 | |
| | | 6 | | 30 | | — | | 37 | | — | | 45 | | — | |
| Output High Z to Low Level (Fig. 7) | $t_{PZL}$ | 2 | | 175 | | — | | 220 | | — | | 265 | | — | ns |
| | | 4.5 | | 35 | | 35 | | 44 | | 44 | | 53 | | 53 | |
| | | 6 | | 30 | | — | | 37 | | — | | 45 | | — | |
| Output High Level to High Z (Fig. 6) | $t_{PHZ}$ | 2 | | 175 | | — | | 220 | | — | | 265 | | — | ns |
| | | 4.5 | | 35 | | 35 | | 44 | | 44 | | 53 | | 53 | |
| | | 6 | | 30 | | — | | 37 | | — | | 45 | | — | |
| Output Low Level to High Z (Fig. 7) | $t_{PLZ}$ | 2 | | 175 | | — | | 220 | | — | | 265 | | — | ns |
| | | 4.5 | | 35 | | 35 | | 44 | | 44 | | 53 | | 53 | |
| | | 6 | | 30 | | — | | 37 | | — | | 45 | | — | |
| Output Transition Time (Fig. 3) | $t_{TLH}$ | 2 | | 60 | | — | | 75 | | — | | 90 | | — | ns |
| | $t_{THL}$ | 4.5 | | 12 | | 12 | | 15 | | 15 | | 18 | | 18 | |
| | | 6 | | 10 | | — | | 13 | | — | | 15 | | — | |



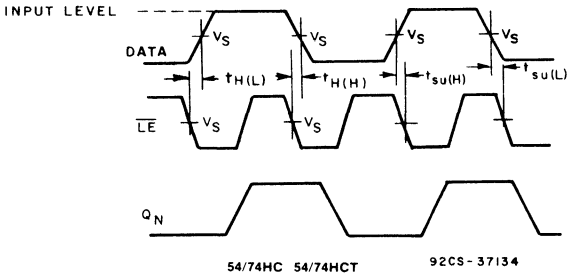

| 54/74HC | 54/74HCT |
|---|---|
| Input Level | Vcc | 3 V |
| Vs | 50% Vcc | 1.3 V |

*Fig. 3 - Data to $Q_n$ output propagation delays and output transition times.*



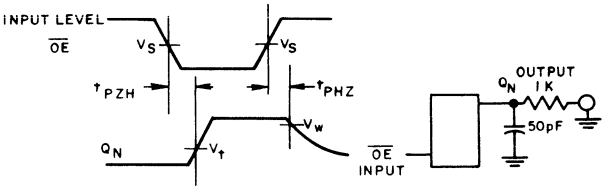

| 54/74HC | 54/74HCT |
|---|---|
| Input Level | Vcc | 3 V |
| Vs | 50% Vcc | 1.3 V |

*Fig. 4 - Latch enable propagation delays.*



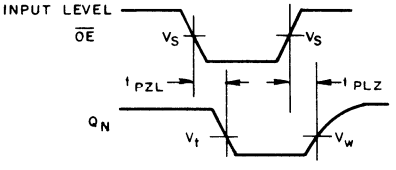

| 54/74HC | 54/74HCT |
|---|---|
| Input Level | Vcc | 3 V |
| Vs | 50% Vcc | 1.3 V |

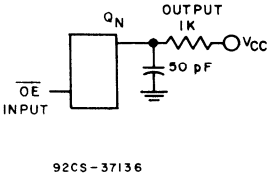
*Fig. 5 - Latch enable pre-requisite times.*




| 54/74HC | 54/74HCT |
|---|---|
| Input Level | Vcc | 3 V |
| Vs | 50% Vcc | 1.3 V |
| Vt | 50% Vcc | 1.3 V |
| Vw | 90% Vcc | 90% Vcc |

*Fig. 6 - Tri-state propagation delays.*



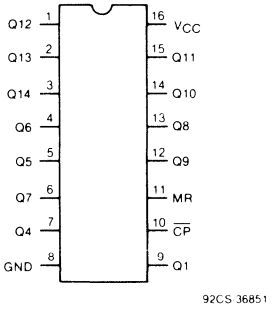




| 54/74HC | 54/74HCT |
|---|---|
| Input Level | Vcc | 3 V |
| Vs | 50% Vcc | 1.3 V |
| Vt | 50% Vcc | 1.3 V |
| Vw | 10% Vcc | 10% Vcc |

*Fig. 7 - Tri-state propagation delays.*

File Number **1484**

**Preliminary Data**




**TERMINAL ASSIGNMENT**

# 14-Stage Binary Counter

**Type Features:**

- *Full static operation*
- *Buffered inputs*
- *Common reset*
- *Negative edge clocking*
- *Typical $F_{MAX}$=50 MHz @ $V_{CC}$=5 V, $C_L$=15 pF*

**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT/HCU: −40 to +85° C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$=20%, $N_{IH}$=30% of $V_{CC}$; @ $V_{CC}$=5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$=0.8 V Max., $V_{IH}$=2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN} \leq 1\ \mu A$ @ $V_{OL}$, $V_{OH}$*

The RCA-CD54/74HC4020 and CD54/74HCT4020 are 14-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each clock pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

The CD54HC4020 and CD54HCT4020 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4020 and CD74HCT4020 are supplied in 16-lead dual-in-line plastic packages (E suffix).

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR -0.5 V < $V_o$ < $V_{CC}$ + 0.5 V) ..... ±25 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±50 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = -55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

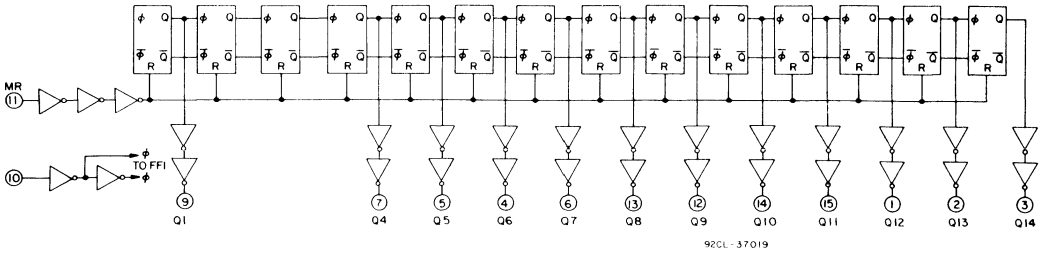



*Fig. 1 - Logic block diagram.*

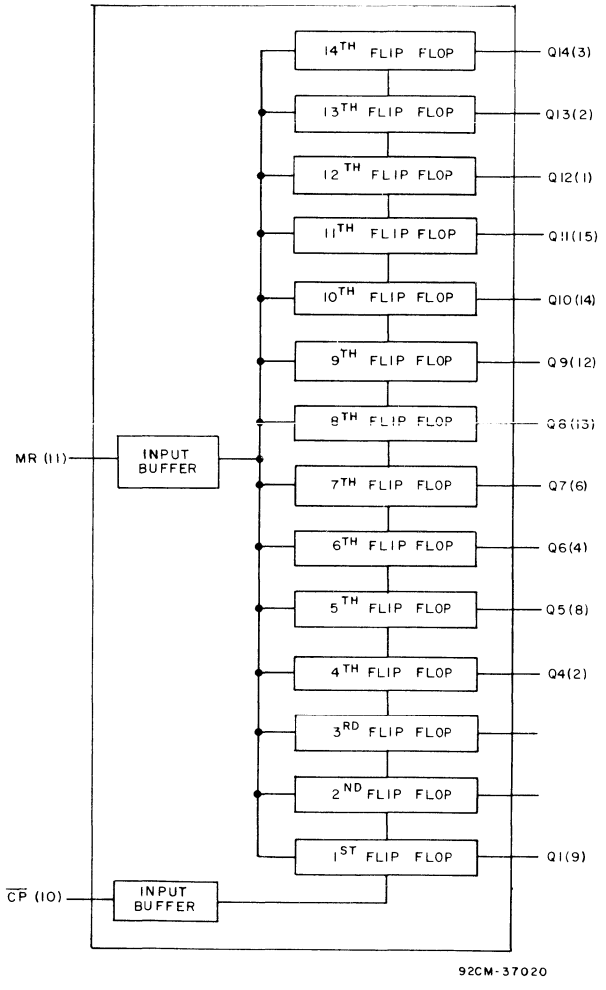



*Fig. 2 - Function diagram.*

**TRUTH TABLE**

| $\overline{CP}$ | MR | Output State |
|---|---|---|
| ⌐ | L | No Change |
| ¬ | L | Advance to next state |
| X | H | All Outputs are low |

H = high level (steady state)
L = low level (steady state)
X = don't care

**RECOMMENDED OPERATING CONDITIONS:**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$=Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{in}$, $V_{out}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times $t_r$,$t_f$ | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC4020/CD54HC4020 | | | | | | | | | | CD74HCT4020/CD54HCT4020 | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC Series | | | 74HC Series | | 54HC Series | | TEST CONS. | | 74HCT/54HCT Series | | | 74HCT Series | | 54HCT Series | | |
| | $V_{IN}$ V | | $V_{CC}$ V | +25°C | | | -40/ +85°C | | -55/ +125°C | | $V_{IN}$ V | $V_{CC}$ V | +25°C | | | -40/ +85°C | | -55/ +125°C | | |
| | | | | Min | Typ | Max | Min | Max | Min | Max | | | Min | Typ | Max | Min | Max | Min | Max | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | — | 4.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | 5.5 | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | — | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | 5.5 | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=-20μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | — | — | — | — | — | — | — | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) -4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | -5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | — | — | — | — | — | — | — | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20 μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | — | — | — | — | — | — | — | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) 4 | — | — | — | — | — | — | — | — | $V_{IL}$ or $V_{IH}$ | — | — | — | — | — | — | — | — | V |
| | | 4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | |
| | | 5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0 4 | | | — | — | — | — | — | — | — | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 8 | — | 80 | — | 160 | $V_{CC}$ or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | μA |

**SWITCHING CHARACTERISTICS ($V_{CC}$=5 V, $T_A$=25° C, Input $t_r$,$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | 54/74HC/HCT | |
|---|---|---|---|
| | | Typical | Units |
| Propagation Delay $\overline{CP}$ to Q1 Output ($C_L$ = 15 pF) | $t_{PLH}$ $t_{PHL}$ | 15 | ns |
| Propagation Delay $Q_n$ to $Q_{n+1}$ ($C_L$ = 15 pF) | $t_{PLH}$ $t_{PHL}$ | 6 | ns |
| Propagation Delay MR to Q1 Output ($C_L$ = 15 pF) | $t_{PHL}$ | 18 | ns |
| Input Capacitance | $C_{in}$ | 3.5 | pF |
| Power Dissipation Capacitance* | $C_{PD}$ | 50 | pF |

*$C_{PD}$ is used to determine the power consumption.
PD = $C_{PD}$ $Vcc^2$ fi + Σ ($C_L$ $Vcc^2$ fi/M) where:
M = $2^1$, $2^4$, $2^5$ . . . $2^{14}$
$C_L$ = output load capacitance
fi = input frequency

**Pre-requisite for Switching Function**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Maximum Clock Frequency | $f_{MAX}$ | 2 | 6 | — | — | — | 5 | — | — | — | 4 | — | — | — | MHz |
| | | 4.5 | 30 | — | 25 | — | 25 | — | 20 | — | 20 | — | 16 | — | |
| | | 6 | 35 | — | — | — | 29 | — | — | — | 23 | — | — | — | |
| Clock Pulse Width (Figure 3) | $t_W$ | 2 | 80 | — | — | — | 100 | — | — | — | 120 | — | — | — | ns |
| | | 4.5 | 16 | — | 20 | — | 20 | — | 25 | — | 24 | — | 30 | — | |
| | | 6 | 14 | — | — | — | 17 | — | — | — | 20 | — | — | — | |
| Reset Removal Time (Figure 4) | $t_{REM}$ | 2 | 50 | — | — | — | 65 | — | — | — | 75 | — | — | — | ns |
| | | 4.5 | 10 | — | 10 | — | 13 | — | 13 | — | 15 | — | 15 | — | |
| | | 6 | 9 | — | — | — | 11 | — | — | — | 13 | — | — | — | |
| Reset Pulse Width (Figure 4) | $t_W$ | 2 | 80 | — | — | — | 100 | — | — | — | 120 | — | — | — | ns |
| | | 4.5 | 16 | — | 20 | — | 20 | — | 25 | — | 24 | — | 30 | — | |
| | | 6 | 14 | — | — | — | 17 | — | — | — | 20 | — | — | — | |

**SWITCHING CHARACTERISTICS ($C_L$=50 pF, Input $t_r$,$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay $\overline{CP}$ to Q1 Output (Figure 3) | $t_{PLH}$ $t_{PHL}$ | 2 | — | 175 | — | — | — | 220 | — | — | — | 265 | — | — | ns |
| | | 4.5 | — | 35 | — | 40 | — | 44 | — | 50 | — | 53 | — | 60 | |
| | | 6 | — | 30 | — | — | — | 37 | — | — | — | 45 | — | — | |
| Propagation Delay $Q_n$ to $Q_{n+1}$ (Figure 3) | $t_{PLH}$ $t_{PHL}$ | 2 | — | 75 | — | — | — | 95 | — | — | — | 100 | — | — | ns |
| | | 4.5 | — | 15 | — | 20 | — | 19 | — | 25 | — | 22 | — | 30 | |
| | | 6 | — | 13 | — | — | — | 16 | — | — | — | 19 | — | — | |
| Propagation Delay MR to Q1 Output (Figure 4) | $t_{PHL}$ | 2 | — | 200 | — | — | — | 250 | — | — | — | 300 | — | — | ns |
| | | 4.5 | — | 40 | — | 45 | — | 50 | — | 56 | — | 60 | — | 68 | |
| | | 6 | — | 34 | — | — | — | 43 | — | — | — | 51 | — | — | |
| Output Transition Time (Figure 3) | $t_{TLH}$ $t_{THL}$ | 2 | — | 75 | — | — | — | 95 | — | — | — | 110 | — | — | ns |
| | | 4.5 | — | 15 | — | 15 | — | 19 | — | 19 | — | 22 | — | 22 | |
| | | 6 | — | 13 | — | — | — | 16 | — | — | — | 19 | — | — | |

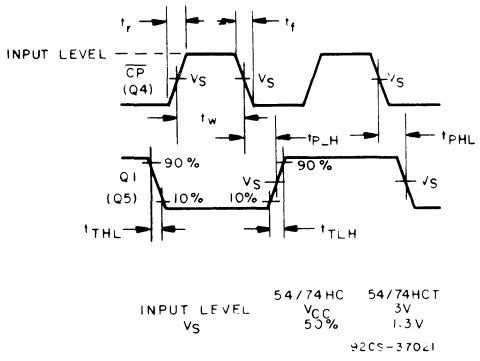



*Fig. 3 - Clock pre-requisite times, propagation delays and output transition times.*

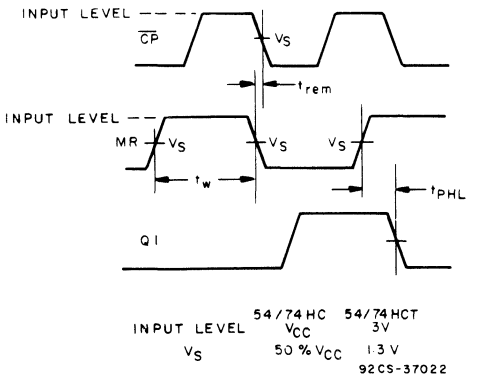
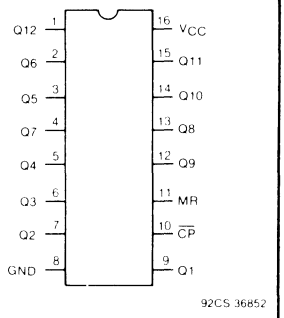



*Fig. 4 - Master Reset pre-requisite and propagation delays.*

**Preliminary Data** File Number **1483**




**TERMINAL ASSIGNMENT**

# 12-Stage Binary Counter

**Type Features:**

- *Full static operation*
- *Buffered inputs*
- *Common reset*
- *Negative edge clocking*
- *Typical $F_{MAX}$=50 MHz @ $V_{CC}$=5 V, $C_L$=15 pF*

**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT/HCU: −40 to +85° C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$=20%, $N_{IH}$=30% of $V_{CC}$; @ $V_{CC}$=5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$=0.8 V Max., $V_{IH}$=2 V Min.*
  *CMOS Input Compatibility*
  *$I_{IN} \leq 1\ \mu A$ @ $V_{OL}$, $V_{OH}$*

The RCA-CD54/74HC4040 and CD54/74HCT4040 are 12-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each clock pulse; a high voltage level on the MR line resets all stages to their zero state. All inputs and outputs are buffered.

The CD54HC4040 and CD54HCT4040 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4040 and CD74HCT4040 are supplied in 16-lead dual-in-line plastic packages (E suffix).

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT CURRENT, $I_{OK}$ (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR $-0.5\ V < V_o < V_{CC} + 0.5$ V) ..... ±25 mA
DC $V_{CC}$ OR GROUND CURRENT, PER PIN ($I_{CC}$): ..... ±50 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For $T_A$ = -55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For $T_A$ = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

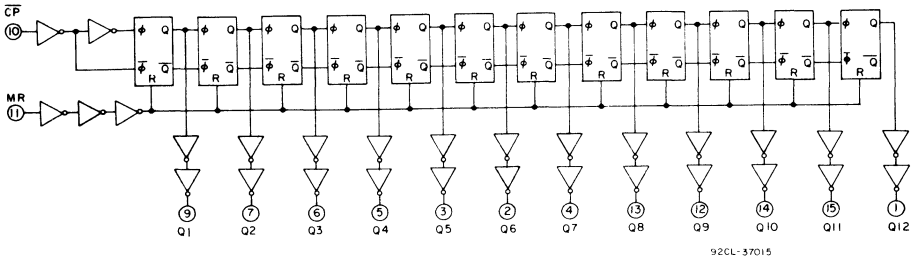



*Fig. 1 - Logic block diagram.*

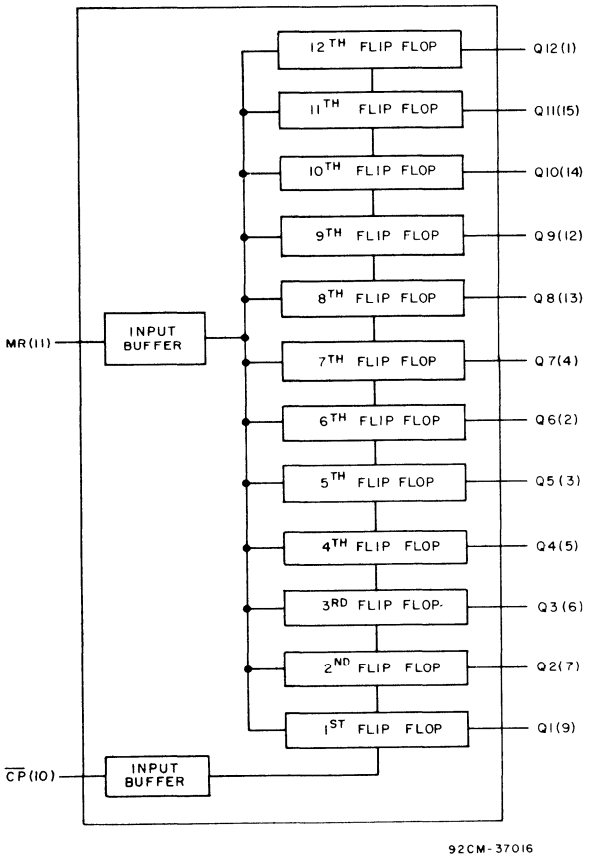



*Fig. 2 - Function diagram.*

**TRUTH TABLE**

| $\overline{CP}$ | MR | Output State |
|---|---|---|
| ⌐‾ | L | No Change |
| ‾⌐ | L | Advance to next state |
| X | H | All Outputs are low |

H = high level (steady state)
L = low level (steady state)
X = don't care

**RECOMMENDED OPERATING CONDITIONS:**
**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$=Full Package Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage $V_{in}$, $V_{out}$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | °C |
| Input Rise and Fall Times $t_r$,$t_f$ | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | ns |
| at 6 V | 0 | 400 | ns |

*Unless otherwise specified, all voltages are referenced to Ground.

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CD74HC4040/CD54HC4040 | | | | | | | | | | CD74HCT4040/CD54HCT4040 | | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC Series | | | 74HC Series | | 54HC Series | | TEST CONS. | | 74HCT/54HCT Series | | | 74HCT Series | | 54HCT Series | | | |
| | $V_{IN}$ V | | $V_{CC}$ V | +25°C | | | -40/ +85°C | | -55/ +125°C | | $V_{IN}$ V | $V_{CC}$ V | +25°C | | | -40/ +85°C | | -55/ +125°C | | | |
| | | | | Min | Typ | Max | Min | Max | Min | Max | | | Min | Typ | Max | Min | Max | Min | Max | | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | — | 4.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | 5.5 | | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.3 | — | 0.3 | — | 0.3 | — | 4.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | 4.5 | — | — | 0.9 | — | 0.9 | — | 0.9 | | 5.5 | | | | | | | | | |
| | | | 6 | — | — | 1.2 | — | 1.2 | — | 1.2 | | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=-20μA | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | — | — | — | — | — | — | — | | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) -4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | -5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | — | — | — | — | — | — | — | | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | $I_O$=20 μA | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | — | — | — | — | — | — | — | | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | — | — | — | — | — | — | — | | |
| TTL Loads (Standard Output) | $V_{IL}$ or $V_{IH}$ | $I_O$ (mA) 4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V |
| | | 5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | — | — | — | — | — | — | — | | |
| Input Leakage Current $I_{IN}$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | $V_{CC}$ or Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | $I_{OUT}$=0 | 6 | — | — | 8 | — | 80 | — | 160 | $V_{CC}$ or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | μA |

**SWITCHING CHARACTERISTICS ($V_{CC}$=5 V, $T_A$=25° C, Input $t_r$,$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | 54/74HC/HCT | |
|---|---|---|---|
| | | Typical | Units |
| Propagation Delay $\overline{CP}$ to Q1 ($C_L$ = 15 pF) | $t_{PLH}$ $t_{PHL}$ | 15 | ns |
| Propagation Delay $Q_n$ to $Q_{n+1}$ ($C_L$ = 15 pF) | $t_{PLH}$ $t_{PHL}$ | 6 | ns |
| Propagation Delay MR to Q1 Output ($C_L$ = 15 pF) | $t_{PHL}$ | 18 | ns |
| Input Capacitance | $C_{in}$ | 3.5 | pF |
| Power Dissipation Capacitance* | $C_{PD}$ | 50 | pF |

*$C_{PD}$ is used to determine the power consumption.
$PD = C_{PD} Vcc^2 fi + \Sigma (C_L Vcc^2 fi/M)$ where:
$M = 2^1, 2^2, 2^3, \ldots 2^{14}$
$C_L$ = output load capacitance
fi = input frequency

**Pre-requisite for Switching Function**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Maximum Clock Frequency | $f_{MAX}$ | 2 | 6 | — | — | — | 5 | — | — | — | 4 | — | — | — | MHz |
| | | 4.5 | 30 | — | 25 | — | 25 | — | 20 | — | 20 | — | 16 | — | |
| | | 6 | 35 | — | — | — | 29 | — | — | — | 23 | — | — | — | |
| Clock Pulse Width (Figure 3) | $t_W$ | 2 | 80 | — | — | — | 100 | — | — | — | 120 | — | — | — | ns |
| | | 4.5 | 16 | — | 20 | — | 20 | — | 25 | — | 24 | — | 30 | — | |
| | | 6 | 14 | — | — | — | 17 | — | — | — | 20 | — | — | — | |
| Reset Removal Time (Figure 4) | $t_{REM}$ | 2 | 50 | — | — | — | 65 | — | — | — | 75 | — | — | — | ns |
| | | 4.5 | 10 | — | 10 | — | 13 | — | 13 | — | 15 | — | 15 | — | |
| | | 6 | 9 | — | — | — | 11 | — | — | — | 13 | — | — | — | |
| Reset Pulse Width (Figure 4) | $t_W$ | 2 | 80 | — | — | — | 100 | — | — | — | 120 | — | — | — | ns |
| | | 4.5 | 16 | — | 20 | — | 20 | — | 25 | — | 24 | — | 30 | — | |
| | | 6 | 14 | — | — | — | 17 | — | — | — | 20 | — | — | — | |

**SWITCHING CHARACTERISTICS ($C_L$=50 pF, Input $t_r$,$t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25° C | | | | -40° C to +85° C | | | | -55° C to +125° C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay $\overline{CP}$ to Q1 Output (Figure 3) | $t_{PLH}$ | 2 | — | 175 | — | — | — | 220 | — | — | — | 265 | — | — | ns |
| | $t_{PHL}$ | 4.5 | — | 35 | — | 40 | — | 44 | — | 50 | — | 53 | — | 60 | |
| | | 6 | — | 30 | — | — | — | 37 | — | — | — | 45 | — | — | |
| Propagation Delay $Q_n$ to $Q_{n+1}$ (Figure 3) | $t_{PLH}$ | 2 | — | 75 | — | — | — | 95 | — | — | — | 100 | — | — | ns |
| | $t_{PHL}$ | 4.5 | — | 15 | — | 20 | — | 19 | — | 25 | — | 22 | — | 30 | |
| | | 6 | — | 13 | — | — | — | 16 | — | — | — | 19 | — | — | |
| Propagation Delay MR to Q1 Output (Figure 4) | $t_{PHL}$ | 2 | — | 200 | — | — | — | 250 | — | — | — | 300 | — | — | ns |
| | | 4.5 | — | 40 | — | 45 | — | 50 | — | 56 | — | 60 | — | 68 | |
| | | 6 | — | 34 | — | — | — | 43 | — | — | — | 51 | — | — | |
| Output Transition Time (Figure 3) | $t_{TLH}$ | 2 | — | 75 | — | — | — | 95 | — | — | — | 110 | — | — | ns |
| | $t_{THL}$ | 4.5 | — | 15 | — | 15 | — | 19 | — | 19 | — | 22 | — | 22 | |
| | | 6 | — | 13 | — | — | — | 16 | — | — | — | 19 | — | — | |

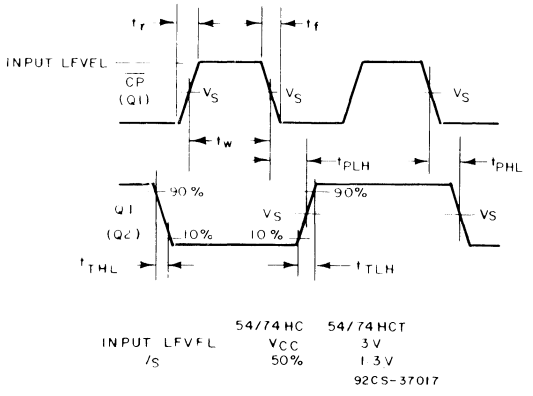



*Fig. 3 - Clock pre-requisite times, propagation delays and output transition times.*

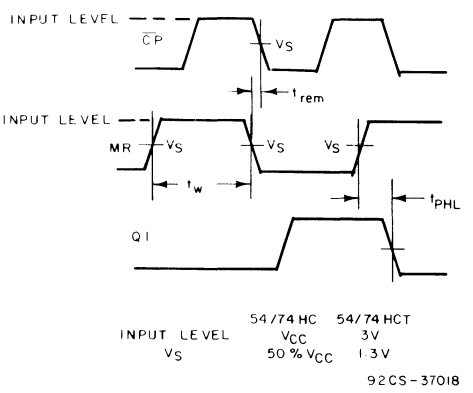


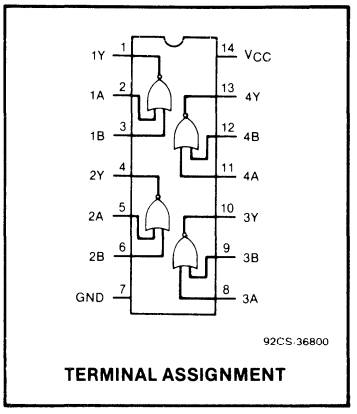

*Fig. 4 - Master Reset pre-requisite and propagation delays.*

# Preview Data

The types shown in the Preview Data section are in the initial stages of design. The data shown are subject to change and RCA reserves the right to alter or discontinue this product without notice. No obligations are assumed for notice of change or future manufacture of these devices. For current information on the status of these types, please contact your local RCA sales office.

# CD54/74HC02
# CD54/74HCT02

## Quad 2-Input NOR Gate



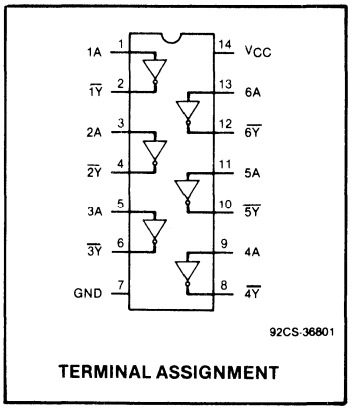

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 8<br>10 | ns<br>ns |

# CD54/74HCU04

## Hex Inverter (Unbuffered)



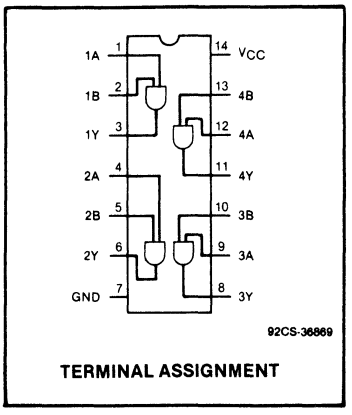

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 4<br>6 | ns<br>ns |

# CD54/74HC08
# CD54/74HCT08

## Quad 2-Input AND Gate



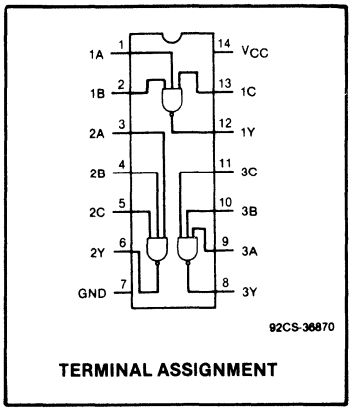

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | | Units |
|---|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF | 7 | 10 | ns |
| | | $C_L$ = 50 pF | 9 | 12 | ns |
| | | | HC08 | HCT08 | |

# CD54/74HC10
# CD54/74HCT10

## Triple 3-Input NAND Gate



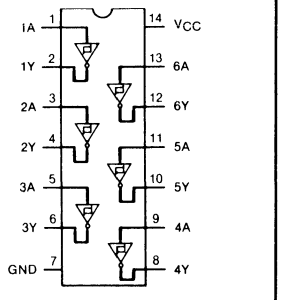

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF | 10 | ns |
| | | $C_L$ = 50 pF | 12 | ns |

# CD54/74HC14
# CD54/74HCT14

## Hex Inverting Schmitt Trigger



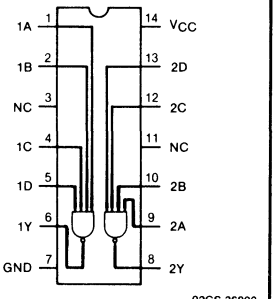

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 10<br>12 | ns<br>ns |

# CD54/74HC20
# CD54/74HCT20

## Dual 4-Input NAND Gate



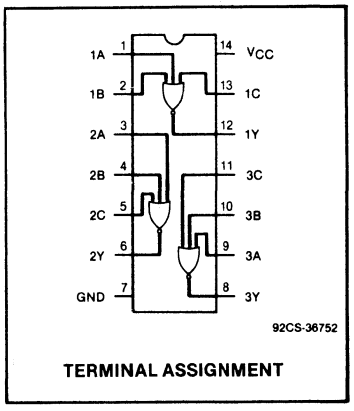

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 15<br>20 | ns<br>ns |

# CD54/74HC27
# CD54/74HCT27

## Triple 3-Input NOR Gate



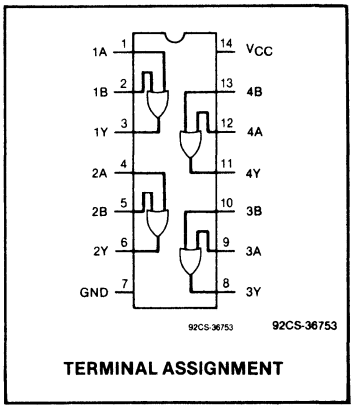

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 10<br>12 | ns<br>ns |

# CD54/74HC32
# CD54/74HCT32

## Quad 2-Input OR Gate



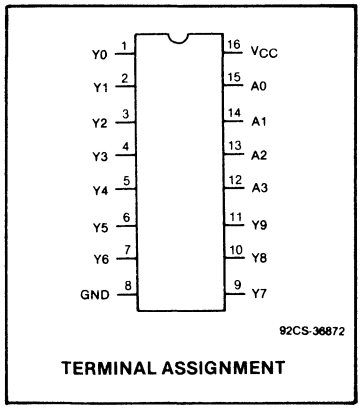

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 7<br>9 | ns<br>ns |

# CD54/74HC42
# CD54/74HCT42

# BCD to Decimal Decoder (1-to-10)




TERMINAL ASSIGNMENT

TRUTH TABLE

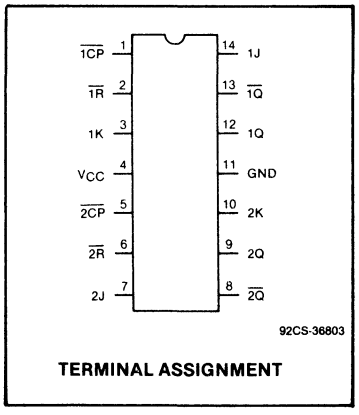
| Inputs | | | | Outputs | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A3 | A2 | A1 | A0 | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 | Y8 | Y9 |
| L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| L | H | L | H | H | H | H | H | H | L | H | H | H | H |
| L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | L | H | H |
| H | L | L | L | H | H | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |
| H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| H | H | H | H | H | H | H | H | H | H | H | H | H | H |

Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 15<br>17 | ns<br>ns |

# CD54/74HC73
# CD54/74HCT73

# Dual J-K Flip-Flop w/Reset
## Negative-Edge Trigger




TERMINAL ASSIGNMENT

TRUTH TABLE

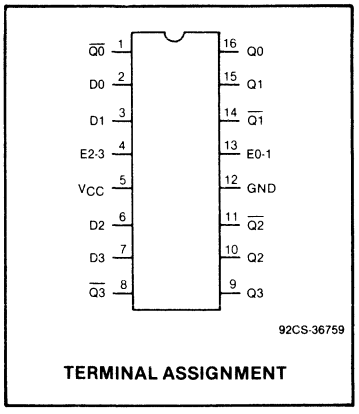
| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| $\overline{R}$ | $\overline{CP}$ | J | K | Q | $\overline{Q}$ |
| L | X | X | X | L | H |
| H | ↓ | L | L | Qo | $\overline{Q}$0 |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | TOGGLE | |
| H | H | X | X | Q0 | $\overline{Q}$0 |

Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Q or $\overline{Q}$ | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC75
# CD54/74HCT75

# Quad Bistable Transparent Latch




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| Inputs | | Outputs | |
|---|---|---|---|
| D | E | Q | $\overline{Q}$ |
| L | H | L | H |
| H | H | H | L |
| X | L | $Q_0$ | $\overline{Q_0}$ |

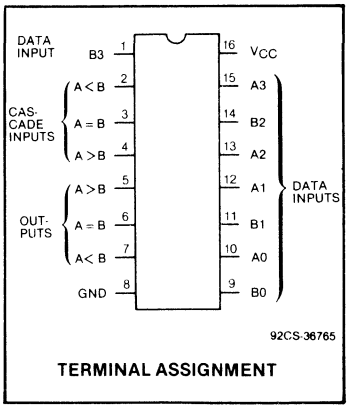
H = High Level
L = Low Level
X = Don't Care
$Q_0$ = The level of Q before the transition of G.

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 10<br>12 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC85
# CD54/74HCT85

# 4-Bit Magnitude Comparator




TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay:<br>Clock to Q | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |

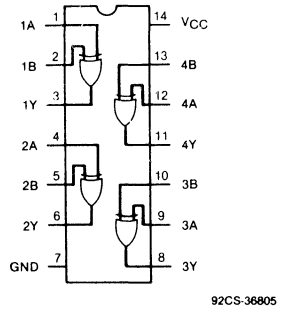
# CD54/74HC85
# CD54/74HCT85

TRUTH TABLE

| Comparing Inputs | | | | Cascading Inputs | | | Outputs | | |
|---|---|---|---|---|---|---|---|---|---|
| A3, B3 | A2, B2 | A1, B1 | A0, B0 | A > B | A < B | A = B | A > B | A < B | A = B |
| A3 > B3 | X | X | X | X | X | X | H | L | L |
| A3 < B3 | X | X | X | X | X | X | L | H | L |
| A3 = B3 | A2 > B2 | X | X | X | X | X | H | L | L |
| A3 = B3 | A2 < B2 | X | X | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 > B1 | X | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 < B1 | X | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 > B0 | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 < B0 | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | L | L | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | H | L | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = A0 | X | X | H | L | L | H |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = A0 | H | H | L | L | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | L | L | H | H | L |

# CD54/74HC86
# CD54/74HCT86

# Quad 2-Input EXCLUSIVE-OR Gate




TERMINAL ASSIGNMENT

TRUTH TABLE

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

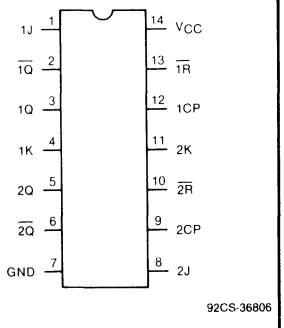
$Y = A \oplus B = \overline{A}B + A\overline{B}$

Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF | 10 | ns |
| | | $C_L$ = 50 pF | 12 | ns |

# CD54/74HC107
# CD54/74HCT107

## Dual J-K Flip-Flop with Reset
### Negative Edge Trigger




TERMINAL ASSIGNMENT

**TRUTH TABLE**

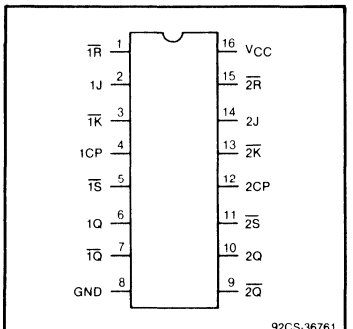
| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{R}$ | CP | J | K | Q | $\overline{Q}$ |
| L | X | X | X | L | H |
| H | ↓ | L | L | QO | QO |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | TOGGLE | |
| H | H | X | X | QO | QO |

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Q or $\overline{Q}$ | $C_L = 15$ pF<br>$C_L = 50$ pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L = 15$ pF<br>$C_L = 50$ pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC109
# CD54/74HCT109

## Dual J-K Flip-Flop with Set and Reset
### Positive-Edge Trigger




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| $\overline{S}$ | $\overline{R}$ | CP | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ↑ | L | L | L | H |
| H | H | ↑ | H | L | TOGGLE | |
| H | H | ↑ | L | H | Q0 | $\overline{Q}$0 |
| H | H | ↑ | H | H | H | L |
| H | H | L | X | X | Q0 | $\overline{Q}$0 |

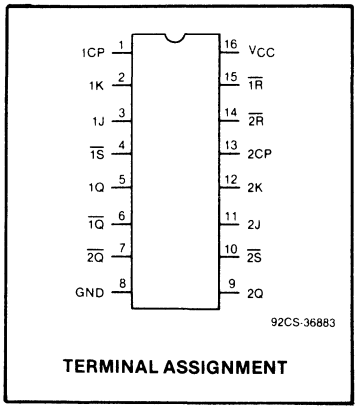
*This is an unstable condition, and is not guaranteed.

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: CP to Q | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC112
# CD54/74HCT112

## Dual J-K Flip-Flop with Set and Reset
### Negative Edge Trigger




TERMINAL ASSIGNMENT

TRUTH TABLE

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| $\overline{S}$ | $\overline{R}$ | CP | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | L* | L* |
| H | H | ↓ | L | L | Q0 | $\overline{Q}$0 |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | TOGGLE | |
| H | H | H | X | X | Q0 | $\overline{Q}$0 |

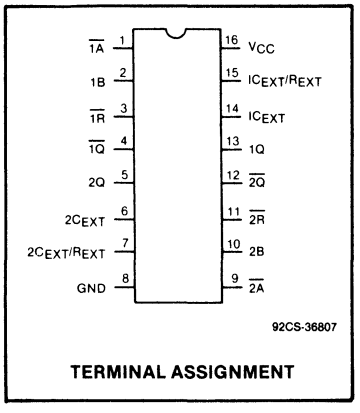
*This is an unstable condition, and is not guaranteed.

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Q | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC123
# CD54/74HCT123
# CD54/74HC221
# CD54/74HCT221
# CD54/74HC423
# CD54/74HCT423

## Dual Retriggerable Monostable Multivibrator with Reset
## Dual Monostable Multivibrator with Reset
## Dual Retriggerable Monostable Multivibrator with Reset




TERMINAL ASSIGNMENT

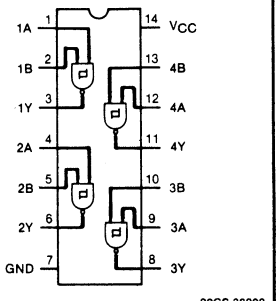
TRUTH TABLE

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{A}$ | B | $\overline{R}$ | Q | $\overline{Q}$ |
| H | X | H | L | H |
| X | L | H | L | H |
| L | ↑ | H | ⎍ | ⎎ |
| ↓ | H | H | ⎍ | ⎎ |
| X | X | L | L | H |

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

# CD54/74HC132
# CD54/74HCT132

# Quad 2-Input NAND Schmitt Trigger



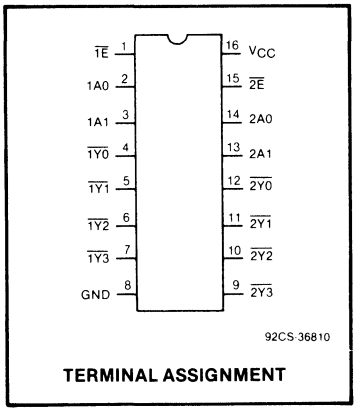

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 8<br>10 | ns<br>ns |

# CD54/74HC139
# CD54/74HCT139

# Dual 2-to-4 Line Decoder/ Demultiplexer




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| ENABLE | SELECT | | | | | |
| E | A1 | A0 | Y0 | Y1 | Y2 | Y3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

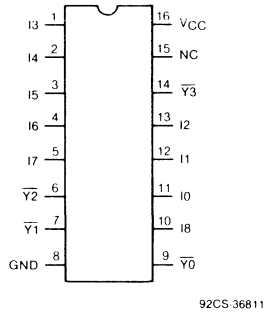
H = high level, L = low level, X = don't care

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Address to Output and Enable to Output | $C_L = 15$ pF<br>$C_L = 50$ pF | 15<br>17 | ns<br>ns |

# CD54/74HC147
# CD54/74HCT147

## 10-to-4 Line-Priority Encoder




TERMINAL ASSIGNMENT

TRUTH TABLE

| Inputs | | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| I0 | I1 | I2 | I3 | I4 | I5 | I6 | I7 | I8 | $\overline{Y3}$ | $\overline{Y2}$ | $\overline{Y1}$ | $\overline{Y0}$ |
| H | H | H | H | H | H | H | H | H | H | H | H | H |
| X | X | X | X | X | X | X | X | L | L | H | H | L |
| X | X | X | X | X | X | X | L | H | L | H | H | H |
| X | X | X | X | X | X | L | H | H | H | L | L | L |
| X | X | X | X | X | L | H | H | H | H | L | L | H |
| X | X | X | X | L | H | H | H | H | H | L | H | L |
| X | X | X | L | H | H | H | H | H | H | L | H | H |
| X | X | L | H | H | H | H | H | H | H | H | L | L |
| X | L | H | H | H | H | H | H | H | H | H | L | H |
| L | H | H | H | H | H | H | H | H | H | H | H | L |

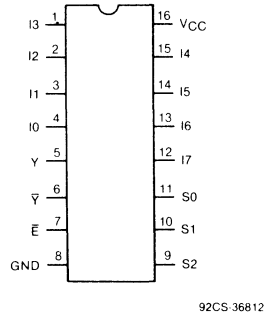
H = High Logic Level, L = Low Logic Level, X = Irrelevant.

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF | 18 | ns |
| | | $C_L$ = 50 pF | 20 | ns |

# CD54/74HC151
# CD54/74HCT151

## 8-Input Multiplexer




TERMINAL ASSIGNMENT

TRUTH TABLE

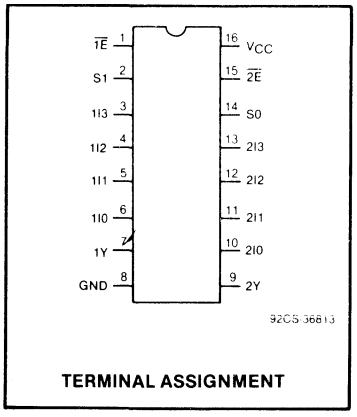
| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| Select | | | Strobe | | |
| S2 | S1 | S0 | $\overline{E}$ | Y | $\overline{Y}$ |
| X | X | X | H | L | $\overline{H}$ |
| L | L | L | L | D0 | $\overline{D0}$ |
| L | L | H | L | D1 | $\overline{D1}$ |
| L | H | L | L | D2 | $\overline{D2}$ |
| L | H | H | L | D3 | $\overline{D3}$ |
| H | L | L | L | D4 | $\overline{D4}$ |
| H | L | H | L | D5 | $\overline{D5}$ |
| H | H | L | L | D6 | $\overline{D6}$ |
| H | H | H | L | D7 | $\overline{D7}$ |

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Select to Y ($\overline{Y}$) | $C_L$ = 15 pF | 20 | ns |
| | | $C_L$ = 50 pF | 22 | ns |
| | Enable to Y ($\overline{Y}$) | $C_L$ = 15 pF | 20 | ns |
| | | $C_L$ = 50 pF | 22 | ns |
| | Data to Y ($\overline{Y}$) | $C_L$ = 15 pF | 15 | ns |
| | | $C_L$ = 50 pF | 17 | ns |

# CD54/74HC153
# CD54/74HCT153

## Dual 4-Input Multiplexer




TERMINAL ASSIGNMENT

TRUTH TABLE

| Select Inputs | | Data Inputs | | | | Enable | Output |
|---|---|---|---|---|---|---|---|
| S1 | S0 | I0 | I1 | I2 | I3 | $\bar{E}$ | Y |
| X | X | X | X | X | X | H | L |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| L | H | X | L | X | X | L | L |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

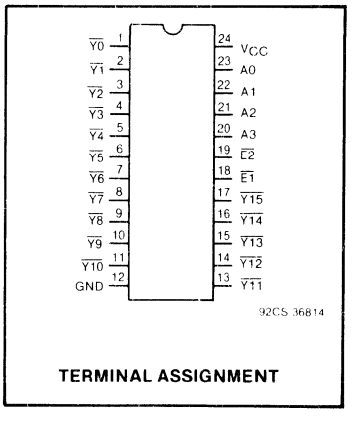
Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care.

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Select to Y ($\bar{Y}$) | $C_L$ = 15 pF | 15 | ns |
| | | $C_L$ = 50 pF | 17 | ns |
| | Enable to Y ($\bar{Y}$) | $C_L$ = 15 pF | 13 | ns |
| | | $C_L$ = 50 pF | 15 | ns |
| | Data to Y ($\bar{Y}$) | $C_L$ = 15 pF | 13 | ns |
| | | $C_L$ = 50 pF | 15 | ns |

# CD54/74HC154
# CD54/74HCT154

## 4-to-16 Line Decoder/ Demultiplexer




TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Address to Output and Enable to Output | $C_L$ = 15 pF | 15 | ns |
| | | $C_L$ = 50 pF | 17 | ns |

# CD54/74HC154
# CD54/74HCT154

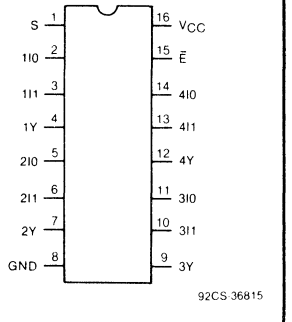
TRUTH TABLE

| INPUTS | | | | | | OUTPUTS | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{E1}$ | $\overline{E2}$ | A3 | A2 | A1 | A0 | $\overline{Y0}$ | $\overline{Y1}$ | $\overline{Y2}$ | $\overline{Y3}$ | $\overline{Y4}$ | $\overline{Y5}$ | $\overline{Y6}$ | $\overline{Y7}$ | $\overline{Y8}$ | $\overline{Y9}$ | $\overline{Y10}$ | $\overline{Y11}$ | $\overline{Y12}$ | $\overline{Y13}$ | $\overline{Y14}$ | $\overline{Y15}$ |
| L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | L | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H |
| L | L | H | H | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| L | L | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | L | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

H = high level, L = low level, X = irrelevant

# CD54/74HC157
# CD54/74HCT157

# Quad 2-Input Multiplexer




TERMINAL ASSIGNMENT

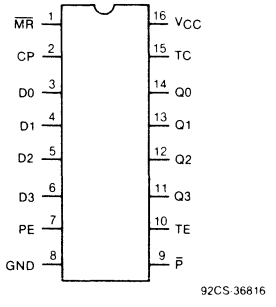
TRUTH TABLE

| INPUTS | | | | OUTPUT Y |
|---|---|---|---|---|
| $\overline{E}$ | S | I0 | I1 | HC/HCT157 |
| H | X | X | X | L |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Data to Output | $C_L = 15$ pF | 10 | ns |
| | | $C_L = 50$ pF | 12 | ns |
| | Select to Output and Strobe to Output | $C_L = 15$pF | 13 | ns |
| | | $C_L = 50$ pF | 15 | ns |

**CD54/74HC160, CD54/74HCT160**
**CD54/74HC161, CD54/74HCT161**
**CD54/74HC162, CD54/74HCT162**
**CD54/74HC163, CD54/74HCT163**




TERMINAL ASSIGNMENT

# Presettable Synchronous Counters

**CD54/74HC/HCT160 BCD Decade Counter, Asynchronous Reset**

**CD54/74HC/HCT161 4-Bit Binary Counter, Asynchronous Reset**

**CD54/74HC/HCT162 BCD Decade Counter, Synchronous Reset**

**CD54/74HC/HCT163 4-Bit Binary Counter, Synchronous Reset**

**Truth Tables**

**HC/HCT160, 161**

| CP | $\overline{MR}$ | PE | TE | $\overline{P}$ | Function |
|---|---|---|---|---|---|
| X | O | X | X | X | Clear |
| X | 1 | 1 | 0 | 1 | Count & TC disabled |
| X | 1 | 0 | 1 | 1 | Count disabled |
| X | 1 | 0 | 0 | 1 | Count & TC disabled |
| ↑ | 1 | X | X | 0 | Load |
| ↑ | 1 | 1 | 1 | 1 | Increment Counter |

**HC/HCT162, 163**

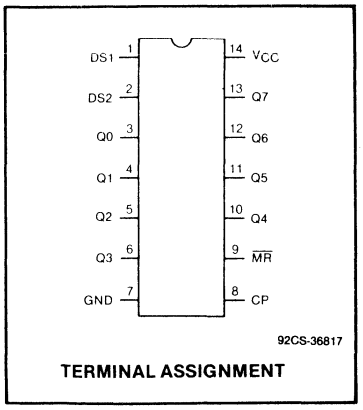
| CP | $\overline{MR}$ | PE | TE | $\overline{P}$ | Function |
|---|---|---|---|---|---|
| ↑ | L | X | X | X | Clear |
| X | H | H | L | H | Count & TC disabled |
| X | H | L | H | H | Count disabled |
| X | H | L | L | H | Count & TC disabled |
| ↑ | H | X | X | L | Load |
| ↑ | H | H | H | H | Increment Counter |

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Q | $C_L = 15$ pF<br>$C_L = 50$ pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L = 15$ pF<br>$C_L = 50$ pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC164
# CD54/74HCT164

## 8-Bit Serial-In/Parallel-Out Shift Register




TERMINAL ASSIGNMENT

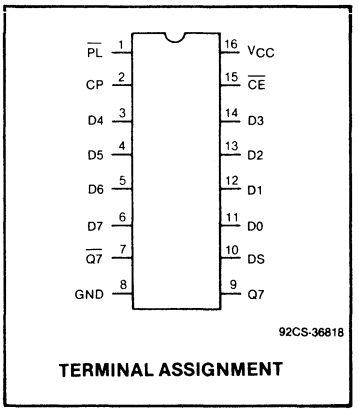
**MODE SELECT—TRUTH TABLE**

| Operating Mode | Inputs | | | | Outputs | | |
|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | CP | DS1 | DS2 | Q0 | Q1 — | Q7 |
| Reset (Clear) | L | X | X | X | L | L — | L |
| Shift | H | ↑ | l | l | L | q0 — | q6 |
| | H | ↑ | l | h | L | q0 — | q0 |
| | H | ↑ | h | l | L | q0 — | q6 |
| | H | ↑ | h | h | H | q0 — | q0 |

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
q = Lower case letters indicate the state of the reference input (or output) one setup time prior to the LOW-to-HIGH clock transition.
x = Don't care.
↑ = LOW-to-HIGH clock transition.

# CD54/74HC165
# CD54/74HCT165

## 8-Bit Parallel-In/Serial-Out Shift Register




TERMINAL ASSIGNMENT

**MODE SELECT — Truth Table**

| Operating Modes | inputs | | | | | $Q_n$ Register | | Outputs | |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{PL}$ | $\overline{CE}$ | CP | DS | D0-D7 | Q0 | Q1-Q6 | Q7 | $\overline{Q7}$ |
| Parallel Load | L | X | X | X | L | L | L - L | L | H |
| | L | X | X | X | H | H | H - H | H | L |
| Serial Shift | H | L | ↑ | l | X | L | q0 - q5 | q6 | $\overline{q6}$ |
| | H | L | ↑ | h | X | H | q0 - q5 | q6 | $\overline{q6}$ |
| Hold "Do Nothing" | H | H | X | X | X | q0 | q1 - q6 | q7 | $\overline{q7}$ |

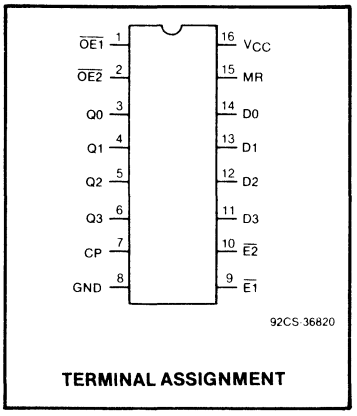
H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
$q_n$ = Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Q or $\overline{Q}$ | $C_L = 15$ pF | 18 | ns |
| | | $C_L = 50$ pF | 20 | ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L = 15$ pF | 60 | MHz |
| | | $C_L = 50$ pF | 50 | MHz |

# CD54/74HC173
# CD54/74HCT173

## Quad-D-Type Flip-Flop, 3-State
### Positive Edge Trigger




**TERMINAL ASSIGNMENT**

**TRUTH TABLE**

| Inputs | | | | Data D | Output Q |
|---|---|---|---|---|---|
| | | Data Enable | | | |
| MR | CP | $\overline{OE1}$ | $\overline{OE2}$ | | |
| H | X | X | X | X | L |
| L | L | X | X | X | $Q_0$ |
| L | ↑ | H | X | X | $Q_0$ |
| L | ↑ | X | H | X | $Q_0$ |
| L | ↑ | L | L | L | L |
| L | ↑ | L | L | H | H |

When either $\overline{OE1}$ or $\overline{OE2}$ (or both) is (are) high the output is disabled to the high-impedance state, however, sequential operation of the flip-flops is not affected.

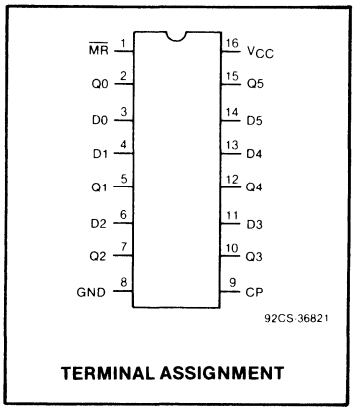
H = high level (steady state)
L = low level (steady state)
↑ = low-to-high level transition
X = don't care (any input including transitions)
$Q_0$ = the level of Q before the indicated steady state input conditions were established.

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Q | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC174
# CD54/74HCT174

## Hex D-Type Flip-Flop with Reset Positive-Edge Trigger




**TERMINAL ASSIGNMENT**

**Truth Table**
**(Each Flip-Flop)**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{MR}$ | CP | D | Q | $\overline{Q}$ |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | $Q_0$ | $\overline{Q_0}$ |

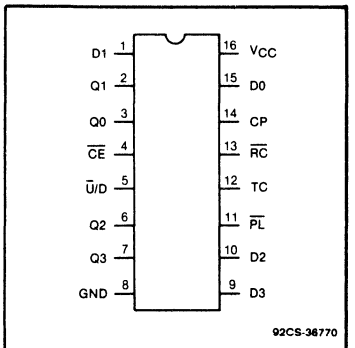
H = High level (steady state).
L = Low level (steady state).
X = Don't Care.
↑ = Transition from low to high level.
$Q_0$ = The level of Q before the indicated steady-state input conditions were established.

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Q | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC190
# CD54/74HCT190

# Presettable Synchronous BCD Decade Up/Down Counter



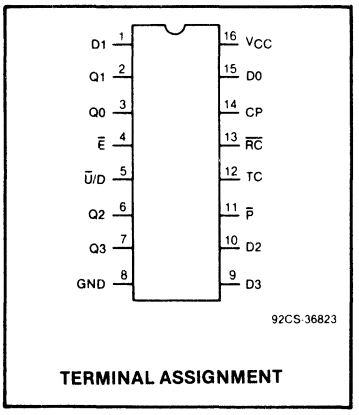

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC191
# CD54/74HCT191

# Presettable Synchronous 4-Bit Binary Up/Down Counter




TERMINAL ASSIGNMENT

**MODE SELECT TABLE**

| Inputs | | | | MODE |
|---|---|---|---|---|
| P | E | U/D | CP | |
| H | L | L | ↑ | Count Up |
| H | L | H | ↑ | Count Down |
| L | X | X | X | Preset (Asyn.) |
| H | H | X | X | No Change (Hold) |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

**RC TRUTH TABLE**

| Inputs | | | Outputs |
|---|---|---|---|
| E | TC* | CP | RC |
| L | H | ⊓ | ⊓ |
| H | X | X | H |
| X | L | X | H |

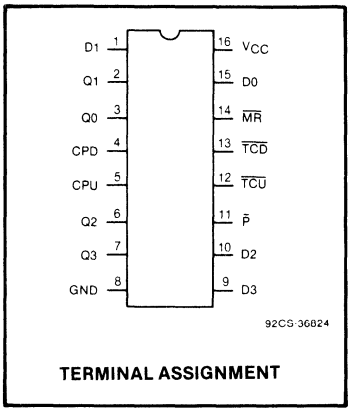
*TC is generated internally.

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC192
# CD54/74HCT192

# Presettable Synchronous BCD Decade Up/Down Counter




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| Count | | | | |
|---|---|---|---|---|
| TCU | TCD | MR | P | Function |
| ↑ | H | L | H | Count Up |
| H | ↑ | L | H | Count Down |
| X | X | H | X | Clear |
| X | X | L | L | Load |

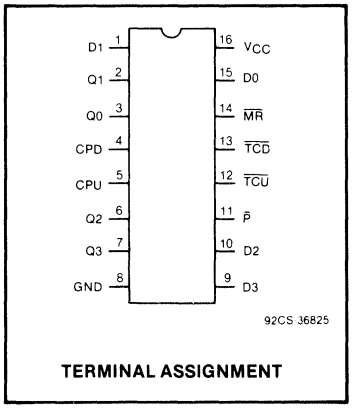
H = High Level  X = Don't care
L = Low Level  ↑ = Transition from low-to-high

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Q | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 24<br>26 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC193
# CD54/74HCT193

# Presettable Synchronous 4-Bit Binary Up/Down Counter




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| Count | | | | |
|---|---|---|---|---|
| Up | Down | MR | P | Function |
| ↑ | H | L | H | Count Up |
| H | ↑ | L | H | Count Down |
| X | X | H | X | Clear |
| X | X | L | L | Load |

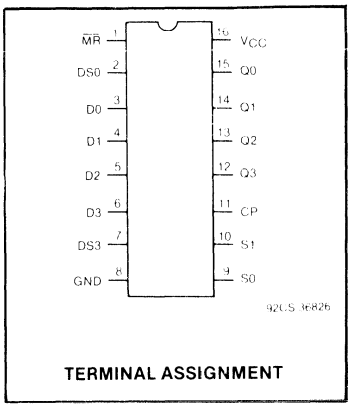
H = High Level  X = Don't care
L = Low Level  ↑ = Transition from low-to-high

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Q | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC194
# CD54/74HCT194

# 4-Bit Bidirectional Universal Shift Register




TERMINAL ASSIGNMENT

**MODE SELECT — TRUTH TABLE**

| Operating Mode | Inputs | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | CP | $\overline{MR}$ | $S_1$ | $S_0$ | DS0 | DS3 | $D_n$ | Q0 | Q1 | Q2 | Q3 |
| Reset (clear) | X | L | X | X | X | X | X | L | L | L | L |
| Hold (do nothing) | X | H | l(b) | l(b) | X | X | X | $q_0$ | $q_1$ | $q_2$ | $q_3$ |
| Shift Left | ↑ | H | h | l(b) | X | l | X | $q_1$ | $q_2$ | $q_3$ | L |
| | ↑ | H | h | l(b) | X | h | X | $q_1$ | $q_2$ | $q_3$ | H |
| Shift Right | ↑ | H | l(b) | h | l | X | X | L | $q_0$ | $q_1$ | $q_2$ |
| | ↑ | H | l(b) | h | h | X | X | H | $q_0$ | $q_1$ | $q_2$ |
| Parallel Load | ↑ | H | h | h | X | X | $d_n$ | $d_0$ | $d_1$ | $d_2$ | $d_3$ |

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
$d_n$ ($q_n$) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

NOTE: b. The HIGH-to-LOW transition of the $S_0$ and $S_1$ inputs on the 54/74194 should only take place while CP is HIGH for conventional operation.

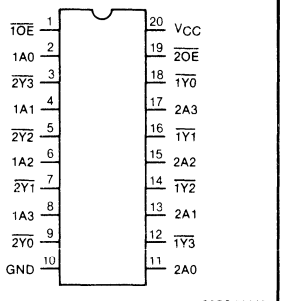
**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Q | $C_L$ = 15 pF | 18 | ns |
| | | $C_L$ = 50 pF | 20 | ns |
| | Reset to Q | $C_L$ = 15 pF | 18 | ns |
| | | $C_L$ = 50 pF | 20 | ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF | 60 | MHz |
| | | $C_L$ = 50 pF | 50 | MHz |

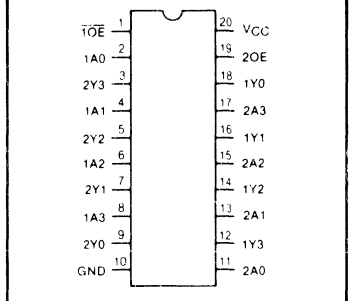
**CD54/74HC240, CD54/74HCT240**
**CD54/74HC241, CD54/74HCT241**
**CD54/74HC244, CD54/74HCT244**

# Octal Buffer/Line Drivers, 3-State

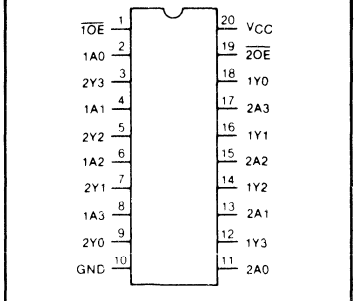
## Inverting and Non-Inverting Outputs




**CD54/74HC, HCT240 Types**
**TERMINAL ASSIGNMENT**




**CD54/74HC, HCT241 Types**
**TERMINAL ASSIGNMENT**




**CD54/74HC,HCT244 Types**
**TERMINAL ASSIGNMENT**

### TRUTH TABLES

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{1OE}$, $\overline{2OE}$ | A | Y |
| L | L | H |
| L | H | L |
| H | X | Z |

(HC/HCT240)

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{1OE}$, $\overline{2OE}$ | A | Y |
| L | L | L |
| L | H | H |
| H | X | Z |

(HC/HCT244)

| INPUTS | | OUTPUT | INPUTS | | OUTPUT |
|---|---|---|---|---|---|
| $\overline{1OE}$ | 1A | 1Y | 2OE | 2A | 2Y |
| L | L | L | L | X | Z |
| L | H | H | H | L | L |
| H | X | Z | H | H | H |

(HCT/HCT241)

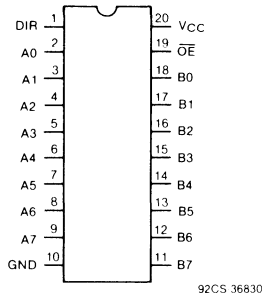
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Data to Output HC/HCT240 only | $C_L$ = 15 pF | 8 | ns |
| | | $C_L$ = 50 pF | 10 | ns |
| | Data to Output HC/HCT241/244 | $C_L$ = 15 pF | 10 | ns |
| | | $C_L$ = 50 pF | 12 | ns |
| | Enable to HiZ | $C_L$ = 15 pF | 12 | ns |
| | | $C_L$ = 50 pF | 15 | ns |
| | Enable from HiZ | $C_L$ = 15 pF | 12 | ns |
| | | $C_L$ = 50 pF | 15 | ns |

# CD54/74HC245
# CD54/74HCT245

## Octal-Bus Transceiver, 3-State




TERMINAL ASSIGNMENT

TRUTH TABLE

| CONTROL INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B DATA TO A BUS |
| L | H | A DATA TO B BUS |
| H | X | ISOLATION |

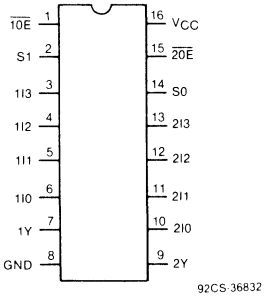
H = high level, L = low level, X = irrelevant

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Data to Output | $C_L = 15$ pF | 10 | ns |
| | | $C_L = 50$ pF | 12 | ns |
| | Enable to HiZ and Enable from HiZ | $C_L = 15$ pF | 12 | ns |
| | | $C_L = 50$ pF | 15 | ns |

# CD54/74HC253
# CD54/74HCT253

## Dual 4-Input Multiplexer, 3-State




TERMINAL ASSIGNMENT

TRUTH TABLE

| SELECT INPUTS | | DATA INPUTS | | | | OUTPUT ENABLE | OUTPUT |
|---|---|---|---|---|---|---|---|
| S1 | S0 | I0 | I1 | I2 | I3 | $\overline{OE}$ | Y |
| X | X | X | X | X | X | H | Z |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| L | H | X | L | X | X | L | L |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

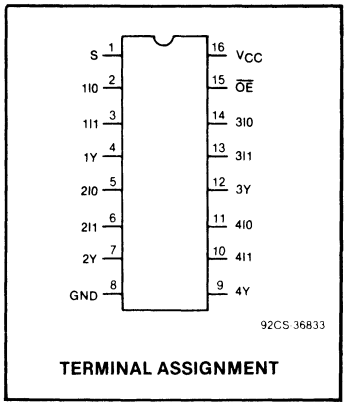
Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant, Z = high impedance (off).

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Data to Output | $C_L = 15$ pF | 13 | ns |
| | | $C_L = 50$ pF | 15 | ns |
| | Select to Output | $C_L = 15$ pF | 15 | ns |
| | | $C_L = 50$ pF | 17 | ns |
| | Enable to HiZ Enable from HiZ | $C_L = 15$ pF | 12 | ns |
| | | $C_L = 50$ pF | 15 | ns |

# CD54/74HC257
# CD54/74HCT257

## Quad 2-Input Multiplexer, 3-State




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| OE | S | I0 | I1 | Y |
| H | X | X | X | Z |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

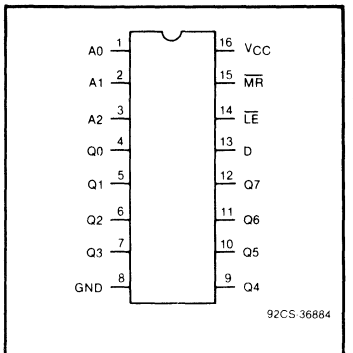
H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Data to Output | $C_L = 15$ pF | 13 | ns |
| | | $C_L = 50$ pF | 15 | ns |
| | Select to Output | $C_L = 15$ pF | 15 | ns |
| | | $C_L = 50$ pF | 17 | ns |
| | Enable to HiZ | $C_L = 15$ pF | 12 | ns |
| | Enable from HiZ | $C_L = 50$ pF | 15 | ns |

# CD54/74HC259
# CD54/74HCT259

## 8-Bit Addressable Latch




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| Inputs | | Output of Addressed Latch | Each Other Output | Function |
|---|---|---|---|---|
| MR | LE | | | |
| H | L | D | $Q_{i0}$ | Addressable Latch |
| H | H | $Q_{i0}$ | $Q_{i0}$ | Memory |
| L | L | D | L | 8-Line Demultiplexer |
| L | H | L | L | Clear |

H = high level, L = low level
D = the level at the data input
$Q_{i0}$ = the level of $Q_i$ (i = 0, 1...7, as appropriate) before the indicated steady-state input conditions were established.

**LATCH SELECTION TABLE**

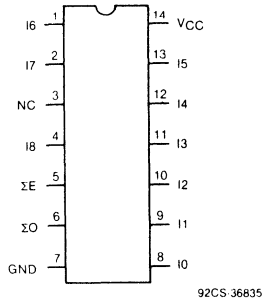
| Select Inputs | | | Latch Addressed |
|---|---|---|---|
| A2 | A1 | A0 | |
| L | L | L | 0 |
| L | L | H | 1 |
| L | H | L | 2 |
| L | H | H | 3 |
| H | L | L | 4 |
| H | L | H | 5 |
| H | H | L | 6 |
| H | H | H | 7 |

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Data to Output | $C_L$ = 15 pF | 15 | ns |
| | | $C_L$ = 50 pF | 17 | ns |

# CD54/74HC280
# CD54/74HCT280

## 9-Bit Odd/Even Parity Generator/Checker




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| NUMBER OF INPUTS 0 THRU 8 THAT ARE HIGH | OUTPUTS | |
|---|---|---|
| | ΣE | ΣO |
| 0, 2, 4, 6, 8 | H | L |
| 1, 3, 5, 7, 9 | L | H |

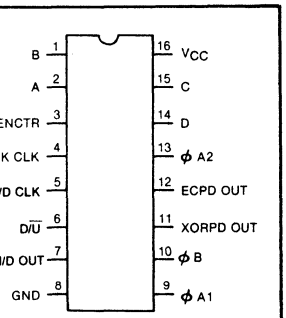
H = high level, L = low level

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L = 15$ pF | 18 | ns |
| | | $C_L = 50$ pF | 20 | ns |

# CD54/74HC297
# CD54/74HCT297

## Digital Phase-Locked-Loop Filter




TERMINAL ASSIGNMENT

**FUNCTION TABLE**
**EDGE-CONTROLLED PHASE DETECTOR**

| φA2 | φB | ECPD OUT |
|---|---|---|
| H or L | ↓ | H |
| ↓ | H or L | L |
| H or L | ↑ | No change |
| ↑ | H or L | No change |

H = steady-state high level
L = steady-state low level
↓ = transition from high to low
↑ = transition from low to high

**K COUNTER FUNCTION TABLE**
**(DIGITAL CONTROL)**

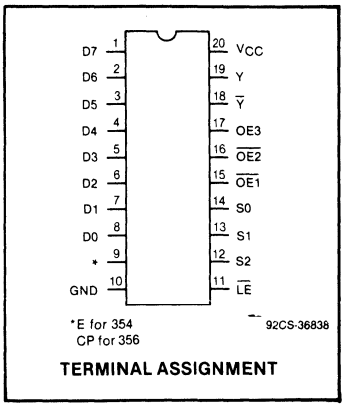
| D | C | B | A | MODULO (K) |
|---|---|---|---|---|
| L | L | L | L | Inhibited |
| L | L | L | H | $2^3$ |
| L | L | H | L | $2^4$ |
| L | L | H | H | $2^5$ |
| L | H | L | L | $2^6$ |
| L | H | L | H | $2^7$ |
| L | H | H | L | $2^8$ |
| L | H | H | H | $2^9$ |
| H | L | L | L | $2^{10}$ |
| H | L | L | H | $2^{11}$ |
| H | L | H | L | $2^{12}$ |
| H | L | H | H | $2^{13}$ |
| H | H | L | L | $2^{14}$ |
| H | H | L | H | $2^{15}$ |
| H | H | H | L | $2^{16}$ |
| H | H | H | H | $2^{17}$ |

**FUNCTION TABLE**
**EXCLUSIVE-OR PHASE DETECTOR**

| φA1 | φB | XORPD OUT |
|---|---|---|
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356

# 8-Input Multiplexer/Register, 3-State




TERMINAL ASSIGNMENT

**CD54/74HC354, CD54/74HCT354 Types**
**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Select to Output | $C_L$ = 15 pF | 32 | ns |
| | | $C_L$ = 50 pF | 34 | ns |
| | $\overline{LE}$ to Output | $C_L$ = 15 pF | 34 | ns |
| | | $C_L$ = 50 pF | 36 | ns |
| | Data to Output | $C_L$ = 15 pF | 29 | ns |
| | | $C_L$ = 50 pF | 31 | ns |
| | Enable to/from HiZ | $C_L$ = 15 pF | 12 | ns |
| | | $C_L$ = 50 pF | 15 | ns |
| | $\overline{OE}$ to Output | $C_L$ = 15 pF | 37 | ns |
| | | $C_L$ = 50 pF | 39 | ns |

**CD54/74HC356, CD54/74HCT356 Types**
**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Output | $C_L$ = 15 pF | 34 | ns |
| | | $C_L$ = 50 pF | 36 | ns |
| | $\overline{OE}$ to Output | $C_L$ = 15 pF | 37 | ns |
| | | $C_L$ = 50 pF | 39 | ns |
| | Select to Output | $C_L$ = 15 pF | 32 | ns |
| | | $C_L$ = 50 pF | 34 | ns |
| | Enable to/from HiZ | $C_L$ = 15 pF | 12 | ns |
| | | $C_L$ = 50 pF | 15 | ns |

**TRUTH TABLE**

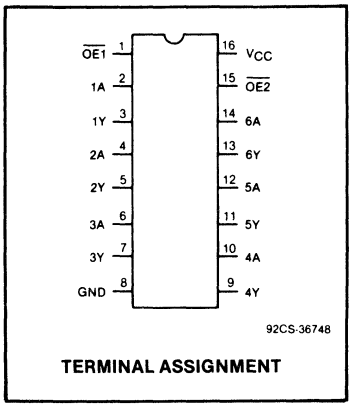
| Inputs | | | | | | | | Outputs | |
|---|---|---|---|---|---|---|---|---|---|
| Select † | | | Enable Data 'HC354 'HCT354 | Clock 'HC356 'HCT356 | Output Enables | | | | |
| S2 | S1 | S0 | $\overline{E}$ | CP | $\overline{OE1}$ | $\overline{OE2}$ | OE3 | $\overline{Y}$ | Y |
| X | X | X | X | X | H | X | X | Z | Z |
| X | X | X | X | X | X | H | X | Z | Z |
| X | X | X | X | X | X | X | L | Z | Z |
| L | L | L | L | ↑ | L | L | H | $\overline{D0}$ | D0 |
| L | L | L | H | H or L | L | L | H | $\overline{D0}_n$ | $D0_n$ |
| L | L | H | L | ↑ | L | L | H | $\overline{D1}$ | D1 |
| L | L | H | H | H or L | L | L | H | $\overline{D1}_n$ | $D1_n$ |
| L | H | L | L | ↑ | L | L | H | $\overline{D2}$ | D2 |
| L | H | L | H | H or L | L | L | H | $\overline{D2}_n$ | $D2_n$ |
| L | H | H | L | ↑ | L | L | H | $\overline{D3}$ | D3 |
| L | H | H | H | H or L | L | L | H | $\overline{D3}_n$ | $D3_n$ |
| H | L | L | L | ↑ | L | L | H | $\overline{D4}$ | D4 |
| H | L | L | H | H or L | L | L | H | $\overline{D4}_n$ | $D4_n$ |
| H | L | H | L | ↑ | L | L | H | $\overline{D5}$ | D5 |
| H | L | H | H | H or L | L | L | H | $\overline{D5}_n$ | $D5_n$ |
| H | H | L | L | ↑ | L | L | H | $\overline{D6}$ | D6 |
| H | H | L | H | H or L | L | L | H | $\overline{D6}_n$ | $D6_n$ |
| H | H | H | L | ↑ | L | L | H | $\overline{D7}$ | D7 |
| H | H | H | H | H or L | L | L | H | $\overline{D7}_n$ | $D7_n$ |

**Notes**
H = high level (steady state)
L = Low level (steady state)
X = irrelevant (any input, including transitions)
Z = high-impedance state (off state)
↑ = transition from low to high level
D0...D7 = the level of steady-state inputs at inputs D0 through D7, respectively, at the time of the low-to-high clock transition in the case of HC356
$D0_n$...$D7_n$ = the level of steady state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control or clock
† This column shows the input address setup with $\overline{LE}$ low

## CD54/74HC365, CD54/74HCT365
## CD54/74HC366, CD54/74HCT366

# Hex Buffer/Line Driver, 3-State

### Non-Inverting and Inverting




TERMINAL ASSIGNMENT

**TRUTH TABLES**

| Inputs | | | Outputs |
|---|---|---|---|
| $\overline{OE}_1$ | $\overline{OE}_2$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| X | H | X | (Z) |
| H | X | X | (Z) |

CD54/74HC, HCT365

| Inputs | | | Outputs |
|---|---|---|---|
| $\overline{OE}_1$ | $\overline{OE}_2$ | A | Y |
| L | L | L | H |
| L | L | H | L |
| X | H | X | (Z) |
| H | X | X | (Z) |

CD54/74HC, HCT366

L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = High impedance (off) state

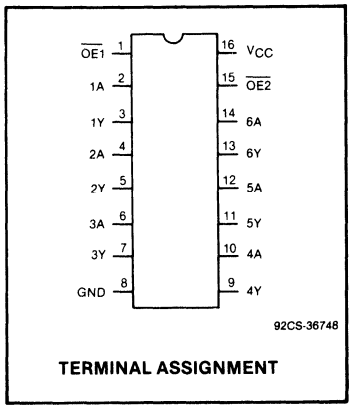
**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: | $C_L = 15$ pF | 8 | ns |
| | Enable to/from HiZ | $C_L = 50$ pF | 10 | ns |

## CD54/74HC367, CD54/74HCT367
## CD54/74HC368, CD54/74HCT368

# Hex Buffer/Line Driver, 3-State

### Non-Inverting and Inverting




TERMINAL ASSIGNMENT

**TRUTH TABLES**

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | L | L |
| L | H | H |
| H | X | (Z) |

CD54/74HC, HCT367

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | L | H |
| L | H | L |
| H | X | (Z) |

CD54/74HC, HCT368

L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.
(Z) = High impedance (off) state.

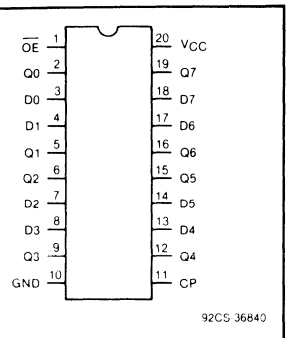
**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: | $C_L = 15$ pF | 8 | ns |
| | Enable to/from HiZ | $C_L = 50$ pF | 10 | ns |

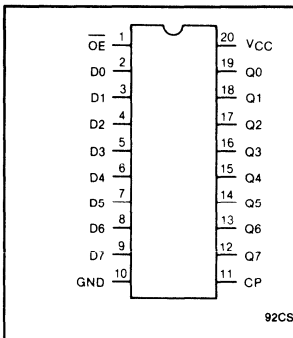
CD54/74HC374, CD54/74HCT374,
CD54/74HC534, CD54/74HCT534
CD54/74HC564, CD54/74HCT564,
CD54/74HC574, CD54/74HCT574

# Octal D-Type Flip-Flop, 3-State

## Positive-Edge Trigger




CD54/74HC, HCT374 Types
TERMINAL ASSIGNMENT

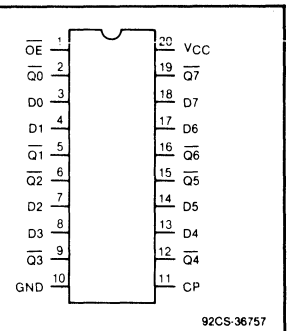



CD54/74HC, HCT574 Types
TERMINAL ASSIGNMENT

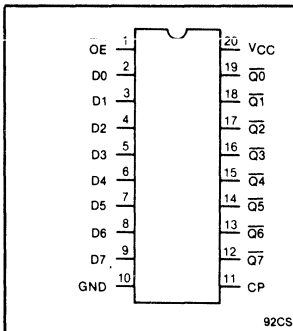
TRUTH TABLES

| Inputs | | | Outputs |
|---|---|---|---|
| $\overline{OE}$ | CP | Dn | Qn |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | Q0 |
| H | X | X | Z |

HC/HCT374, 574




CD54/74HC, HCT534 Types
TERMINAL ASSIGNMENT




CD54/74HC, HCT564 Types
TERMINAL ASSIGNMENT

| Inputs | | | Outputs |
|---|---|---|---|
| $\overline{OE}$ | CP | Dn | Qn |
| L | ↑ | H | L |
| L | ↑ | L | H |
| L | L | X | Q0 |
| H | X | X | Z |

HC/HCT534, 564

H = high level (steady state)
L = low level (steady state)
X = don't care
↑ = transition from low to high level
Q0 = the level of Q before the indicated steady-state input conditions were established.
Z = high impedance

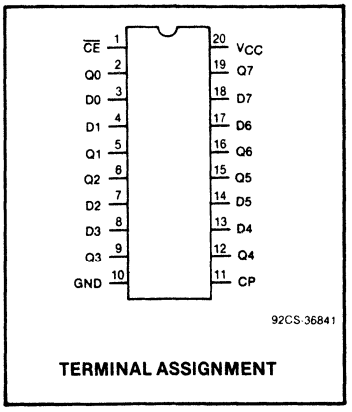
**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5\,V$, $t_r, t_f = 6\,ns$**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Date | $C_L = 15\,pF$ | 18 | ns |
| | | $C_L = 50\,pF$ | 20 | ns |
| | Enable to HiZ<br>Enable from HIZ | $C_L = 15\,pF$ | 12 | ns |
| | | $C_L = 50\,pF$ | 15 | ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L = 15\,pF$ | 60 | MHz |
| | | $C_L = 50\,pF$ | 50 | MHz |

# CD54/74HC377
# CD54/74HCT377

# Octal D-Type Flip-Flop with Data Enable

## Positive-Edge Trigger




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| Operating Mode | Inputs | | | Outputs |
|---|---|---|---|---|
| | CP | $\overline{CE}$ | $D_n$ | $Q_n$ |
| Load "1" | ↑ | l | h | H |
| Load "0" | ↑ | l | l | L |
| Hold (do nothing) | ↑ | h | X | no change |
| | X | H | X | no change |

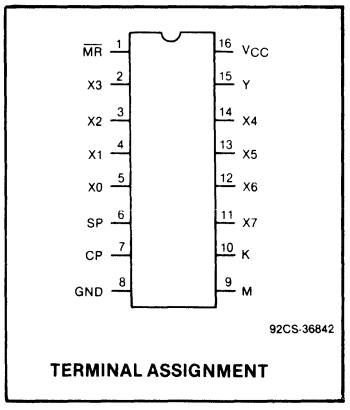
H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Q | $C_L$ = 15 pF | 18 | ns |
| | | $C_L$ = 50 pF | 20 | ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF | 60 | MHz |
| | | $C_L$ = 50 pF | 50 | MHz |

# CD54/74HC384
# CD54/74HCT384

# 8-Bit Serial/Parallel Two's Compliment Multiplier




**TERMINAL ASSIGNMENT**

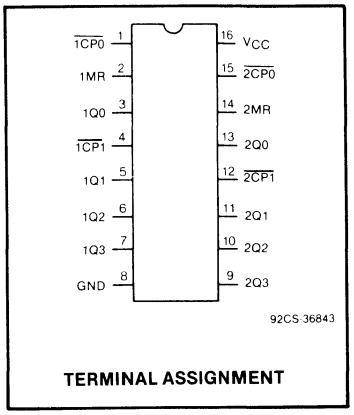
**TRUTH TABLE**

| Inputs | | | | | | Internal | Outputs | Function |
|---|---|---|---|---|---|---|---|---|
| $\overline{MR}$ | CP | K | M | X | Y | $Y_{a-1}$ | SP | |
| | | L | L | | | | | Most Significant Multiplier Device |
| | | CS | H | | | | | Devices Cascaded in Multiplier String |
| L | | | | OP | | L | L | Load New Multiplicand and Clear Internal Sum and Carry Registers |
| H | | | | | | | | Device Enabled |
| H | ⎍ | | | | L | L | AR | Shift Sum Register |
| H | ⎍ | | | | L | H | AR | Add Multiplicand to Sum Register and Shift |
| H | ⎍ | | | | H | L | AR | Subtract Multiplicand from Sum Register and Shift |
| H | ⎍ | | | | H | H | AR | Shift Sum Register |

⎍ = LOW-to-HIGH transition
CS = Connected to SP output of high order device
OP = X latches open for new data i = 0.7
AR = Output as required per Booth's algorithm

# CD54/74HC390
# CD54/74HCT390

# Dual Decade Ripple Counter



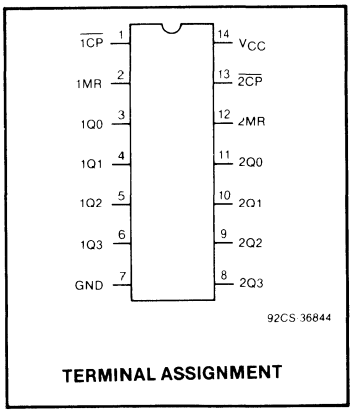

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to $Q_0$ | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC393
# CD54/74HCT393

# Dual 4-Bit Binary Ripple Counter



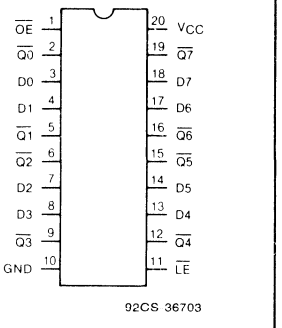

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to $Q_0$ | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

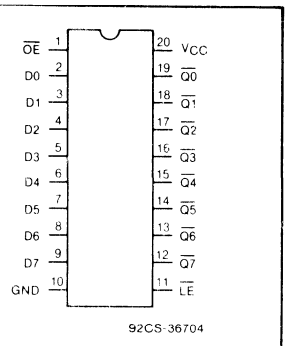
**CD54/74HC533, CD54/74HCT533**
**CD54/74HC563, CD54/74HCT563,**
**CD54/74HC573, CD54/74HCT573**

# Octal Transparent Latch, 3-State



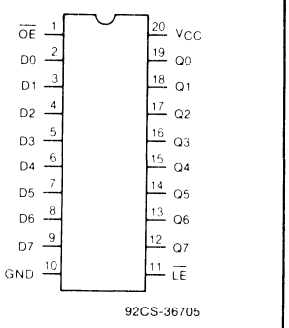

92CS 36703

**CD54/74HC533, CD54/74HCT533**
**TERMINAL ASSIGNMENT**




92CS-36704

**CD54/74HC563, CD54/74HCT563**
**TERMINAL ASSIGNMENT**




92CS-36705

**CD54/74HC573, CD54/74HCT573**
**TERMINAL ASSIGNMENT**

## TRUTH TABLES

| Inputs | | | Outputs |
|---|---|---|---|
| $\overline{OE}$ | $\overline{LE}$ | Dn | Qn |
| L | H | H | L |
| L | H | L | H |
| L | L | X | Q0 |
| H | X | X | Z |

HC/HCT533, 563

| Inputs | | | Outputs |
|---|---|---|---|
| $\overline{OE}$ | $\overline{LE}$ | Dn | Qn |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q0 |
| H | X | X | Z |

HC/HCT573

H = high level (steady state)
L = low level (steady state)
X = don't care
Q0 = the level of Q before the indicated steady-state input conditions were established
Z = high impedance

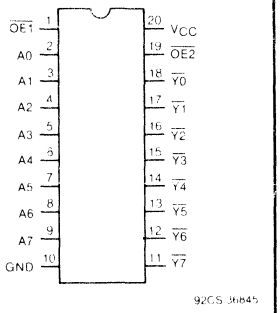
**Dynamic Electrical Characteristics @ $T_A = 25\,°C$, $V_{CC} = 5\,V$, $t_r, t_f = 6\,ns$**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Data to Q | $C_L = 15\,pF$ | 13 | ns |
| | | $C_L = 50\,pF$ | 15 | ns |
| | LE to Q | $C_L = 15\,pF$ | 18 | ns |
| | | $C_L = 50\,pF$ | 20 | ns |
| | Enable to HiZ | $C_L = 15\,pF$ | 12 | ns |
| | Enable from HiZ | $C_L = 50\,pF$ | 15 | ns |

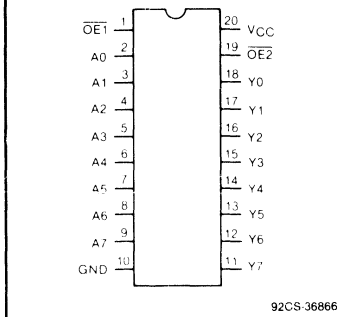
CD54/74HC540, CD54/74HCT540
CD54/74HC541, CD54/74HCT541

# Octal Buffer/Line Driver, 3-State

## Inverting and Non-Inverting Outputs




CD54/74HC,HCT540 TYPES
TERMINAL ASSIGNMENT




CD54/74HC,HCT541 TYPES
TERMINAL ASSIGNMENT

**TRUTH TABLE**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | D | HC/ HCT540 | HC/ HCT541 |
| *L* | *L* | *H* | *L* | *H* |
| *H* | *X* | *X* | *Z* | *Z* |
| *X* | *H* | *X* | *Z* | *Z* |
| *L* | *L* | *L* | *H* | *L* |

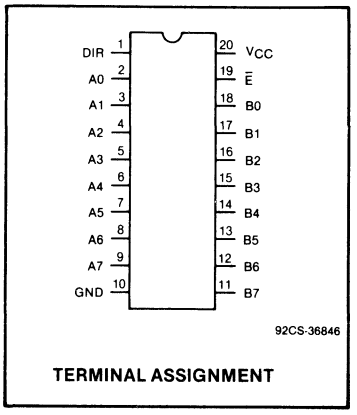
*H* = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High impedance

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output (CD54/74HC, HCT540) | $C_L = 15$ pF | 8 | ns |
| | | $C_L = 50$ pF | 10 | ns |
| | Input to Output (CD54/74HC, HCT541) | $C_L = 15$ pF | 10 | ns |
| | | $C_L = 50$ pF | 12 | ns |
| | Enable to HiZ | $C_L = 15$ pF | 12 | ns |
| | Enable from HiZ | $C_L = 50$ pF | 15 | ns |

# Octal Bus Transceiver, 3-State

## Inverting and True/Inverting




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| CONTROL INPUTS | | OPERATION | |
|---|---|---|---|
| $\bar{E}$ | DIR | HC/HCT640 | HC/HCT643 |
| L | L | $\bar{B}$ DATA TO A BUS | B DATA TO A BUS |
| L | H | $\bar{A}$ DATA TO B BUS | $\bar{A}$ DATA TO B BUS |
| H | X | ISOLATION | ISOLATION |

H = High level, L = Low level, X = Irrelevant

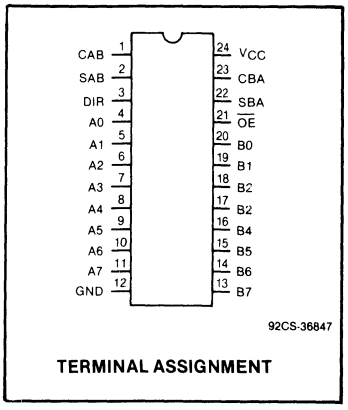
**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output (Type 640 only) | $C_L = 15$ pF | 10 | ns |
| | | $C_L = 50$ pF | 12 | ns |
| | Input to Output ($\bar{A}$ to B) (Type 643 only) | $C_L = 15$ pF | 10 | ns |
| | | $C_L = 50$ pF | 12 | ns |
| | Input to Output (B to A) (Type 643 only) | $C_L = 15$ pF | 8 | ns |
| | | $C_L = 50$ pF | 10 | ns |
| | Enable to HiZ and Enable from HiZ | $C_L = 15$ pF | 12 | ns |
| | | $C_L = 50$ pF | 15 | ns |

**CD54/74HC646, CD54/74HCT646**
**CD54/74HC648, CD54/74HCT648**

# Octal Bus Transceiver/ Register, 3-State

## Non-Inverting and Inverting




**TERMINAL ASSIGNMENT**

**TRUTH TABLE**

| INPUTS | | | | | | DATA I/O* | | OPERATION OR FUNCTION | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CAB | CBA | SAB | SBA | A0 THRU A7 | B0 THRU B7 | HC/HCT646 | HC/HCT648 |
| H | X | H or L | H or L | X | X | Input | Input | Isolation | Isolation |
| H | X | ↑ | ↑ | X | X | | | Store A and B Data | Store A and B Data |
| L | L | X | X | X | L | Output | Input | Real Time B Data to A Bus | Real Time $\overline{B}$ Data to A Bus |
| L | L | X | X | X | H | | | Stored B Data to A Bus | Stored $\overline{B}$ Data to A Bus |
| L | H | X | X | L | X | Input | Output | Real Time A Data to B Bus | Real Time $\overline{A}$ Data to B Bus |
| L | H | H or L | X | H | X | | | Stored A Data to B Bus | Stored $\overline{A}$ Data to B Bus |

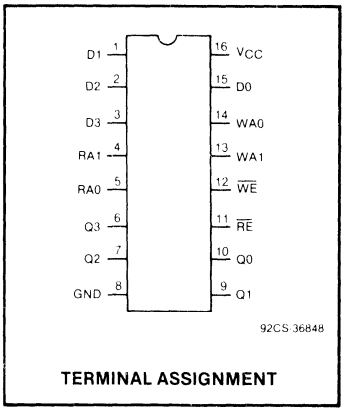
H = high level, L = low level, X = irrelevant ↑ = low-to-high-level transition
*The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Bus | $C_L = 15$ pF | 23 | ns |
| | | $C_L = 50$ pF | 25 | ns |
| | Bus to Bus | $C_L = 15$ pF | 13 | ns |
| | | $C_L = 50$ pF | 15 | ns |
| | Select to Bus | $C_L = 15$ pF | 20 | ns |
| | | $C_L = 50$ pF | 22 | ns |
| | Enable (Direction) to Hi Z | $C_L = 15$ pF | 17 | ns |
| | Enable (Direction) from Hi Z | $C_L = 50$ pF | 20 | ns |

# CD54/74HC670
# CD54/74HCT670

# 4 x 4 Register File, 3-State




TERMINAL ASSIGNMENT

**WRITE MODE SELECT TABLE**

| Operating Mode | Inputs | | Internal Latches[a] |
|---|---|---|---|
| | WE | $D_n$ | |
| Write Data | L | L | L |
| | L | H | H |
| Data Latched | H | X | no change |

NOTE
a. The Write Address (WA0 & WA1) to the "internal latches" must be stable while $\overline{WE}$ is LOW for conventional operation.

**READ MODE SELECT TABLE**

| Operating Mode | Inputs | | Outputs |
|---|---|---|---|
| | $\overline{RE}$ | Internal Latches[b] | $Q_n$ |
| Read | L | L | L |
| | L | H | H |
| Disabled | H | X | (Z) |

NOTE
b. The Read Address (RA0 & RA1) changes to select the "internal latches" are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

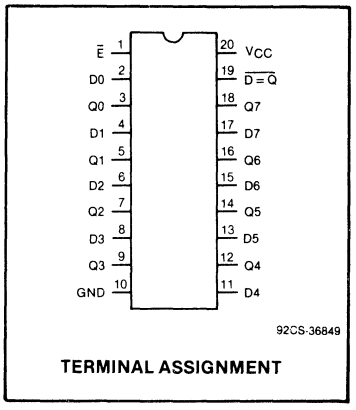
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance "off" state

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Read to Output | $C_L$ = 15 pF | 23 | ns |
| | | $C_L$ = 50 pF | 25 | ns |
| | Write to Output | $C_L$ = 15 pF | 34 | ns |
| | | $C_L$ = 50 pF | 36 | ns |
| | Data to Output | $C_L$ = 15 pF | 28 | ns |
| | | $C_L$ = 50 pF | 30 | ns |

# CD54/74HC688
# CD54/74HCT688

## 8-Bit Magnitude Comparator




TERMINAL ASSIGNMENT

**TRUTH TABLE**

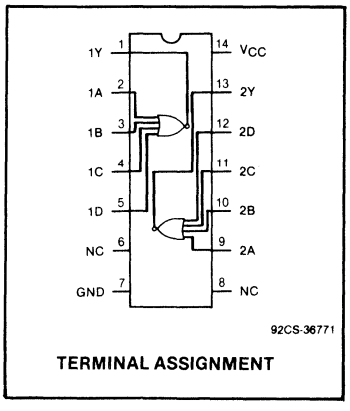
| INPUTS | | |
|---|---|---|
| DATA D, Q | ENABLE $\overline{E}$ | $\overline{D = Q}$ |
| D = Q | L | L |
| D > Q | L | H |
| D < Q | L | H |
| X | H | H |

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay:<br>Input P to Output<br>Input Q to Output<br>Input G to Output | <br>$C_L = 15$ pF<br>$C_L = 50$ pF | <br>13<br>15 | <br>ns<br>ns |

# CD54/74HC4002
# CD54/74HCT4002

## Dual 4-Input NOR Gate



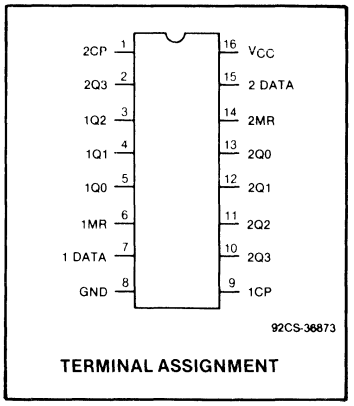

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay:<br>Input to Output | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 10<br>12 | ns<br>ns |

# CD54/74HC4015
# CD54/74HCT4015

# Dual 4-Bit Serial-In/Parallel-Out Shift Register



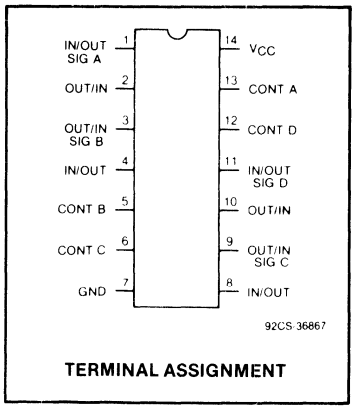

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: CP to $Q_n$ | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC4016, CD54/74HCT4016
# CD54/74HC4066, CD54/74HCT4066

# Quad Bilateral Switch




TERMINAL ASSIGNMENT

TRUTH TABLE

| CP▲ | D | MR | $Q_o$ | $Q_n$ |
|---|---|---|---|---|
| ⌐⌐ | 0 | 0 | 0 | $Q_n - 1$ |
| ⌐⌐ | 1 | 0 | 1 | $Q_n - 1$ |
| ⌐⌐ | X | 0 | $Q_o$ | $Q_n$ (No Change) |
| X | X | 1 | 0 | 0 |

▲ = LEVEL CHANGE
X = DON'T CARE CASE

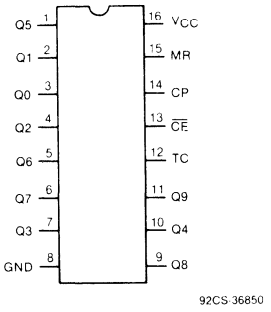
**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Sw. Input to Output | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 3<br>5 | ns<br>ns |
| | Turn-On Delay and Turn-Off Delay* | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 6<br>8 | ns<br>ns |
| $R_{ON}$ | On-State Resistance | $R_L$ = 1 KΩ<br>$C_L$ = 50 pF | 200(4016)<br>50(4066) | Ω<br>Ω |

*Turn-On measured 50% to 50%, Turn-Off measured 50% to 10%.

# CD54/74HC4017, CD54/74HCT4017

## Johnson Decade Counter with 10 Decoded Outputs




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| CP | $\overline{CE}$ | MR | Decode Output = Qn |
|---|---|---|---|
| L | X | L | n |
| X | H | L | n |
| X | X | H | Q0 |
| ↑ | L | L | n + 1 |
| ↓ | X | L | n |
| X | ↑ | L | n |
| H | ↓ | L | n + 1 |

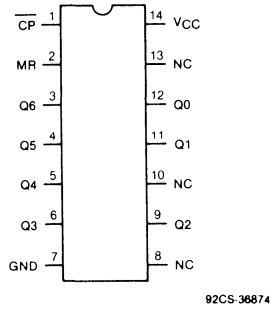
X = Don't Care If n < 5 Carry = H Otherwise = L

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: CP to Qn | $C_L$ = 15 pF | 28 | ns |
| | | $C_L$ = 50 pF | 30 | ns |
| | CP to TC | $C_L$ = 15 pF | 28 | ns |
| | | $C_L$ = 50 pF | 30 | ns |
| | MR to Qn | $C_L$ = 15 pF | 22 | ns |
| | | $C_L$ = 50 pF | 24 | ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF | 60 | MHz |
| | | $C_L$ = 50 pF | 50 | MHz |

# CD54/74HC4024 CD54/74HCT4024

## 7-Stage Binary Ripple Counter




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| CLOCK | RESET | OUTPUT STATE |
|---|---|---|
| ↑ | L | No Change |
| ↓ | L | Advance to next state |
| X | H | All Outputs are low |

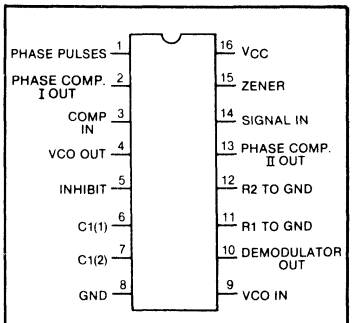
H = high level (steady state)
L = low level (steady state)
X = don't care

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: CP to $Q_1$ | $C_L$ = 15 pF | 18 | ns |
| | | $C_L$ = 50 pF | 20 | ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF | 60 | MHz |
| | | $C_L$ = 50 pF | 50 | MHz |

# CD54/74HC4046
# CD54/74HCT4046

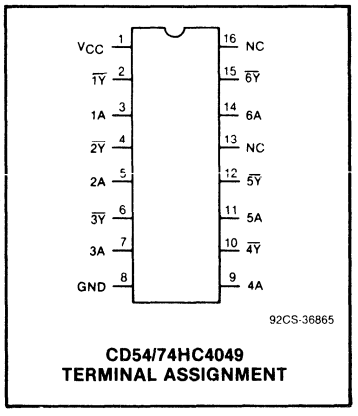
## Phase-Locked Loop with VCO



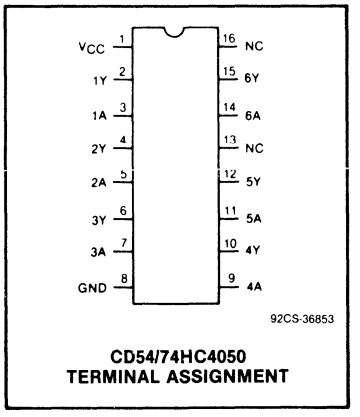

TERMINAL ASSIGNMENT

# CD54/74HC4049
# CD54/74HC4050

## Hex High-to-Low Level Shifter
### Inverting and Non-Inverting




CD54/74HC4049
TERMINAL ASSIGNMENT




CD54/74HC4050
TERMINAL ASSIGNMENT

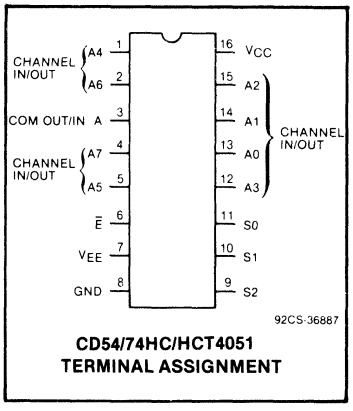
**TRUTH TABLE**

| Type | Data A | Output Y |
|---|---|---|
| CD54/74HC4049 | 0 | 1 |
| | 1 | 0 |
| CD54/74HC4050 | 0 | 0 |
| | 1 | 1 |

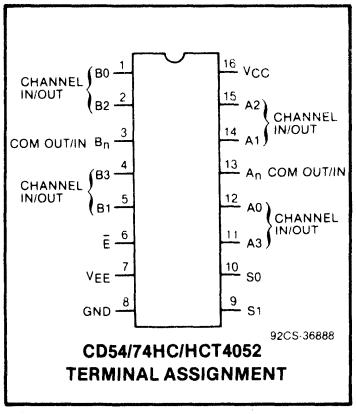
**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: (CD54/74HC4049) | $C_L$ = 15 pF | 8 | ns |
| | | $C_L$ = 50 pF | 10 | ns |
| | (CD54/74HC4050) | $C_L$ = 15 pF | 6 | ns |
| | | $C_L$ = 50 pF | 8 | ns |

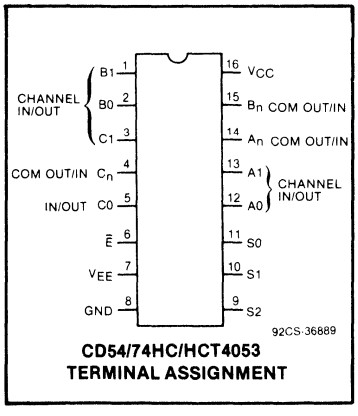
## CD54/74HC/HCT4051 — 8-Channel
## CD54/74HC/HCT4052 — Dual 4-Channel
## CD54/74HC/HCT4053 — Triple 2-Channel




**CD54/74HC/HCT4051**
**TERMINAL ASSIGNMENT**




**CD54/74HC/HCT4052**
**TERMINAL ASSIGNMENT**




**CD54/74HC/HCT4053**
**TERMINAL ASSIGNMENT**

### TRUTH TABLES

| INPUT STATES | | | | "ON" CHANNEL(S) |
|---|---|---|---|---|
| ENABLE | S2 | S1 | S0 | |
| **CD54/74HC/HCT4051** | | | | |
| 0 | 0 | 0 | 0 | A0 |
| 0 | 0 | 0 | 1 | A1 |
| 0 | 0 | 1 | 0 | A2 |
| 0 | 0 | 1 | 1 | A3 |
| 0 | 1 | 0 | 0 | A4 |
| 0 | 1 | 0 | 1 | A5 |
| 0 | 1 | 1 | 0 | A6 |
| 0 | 1 | 1 | 1 | A7 |
| 1 | X | X | X | NONE |
| **CD54/74HC/HCT4052** | | | | |
| **ENABLE** | **S1** | **S0** | | |
| 0 | 0 | 0 | | A0, B0 |
| 0 | 0 | 1 | | A1, B1 |
| 0 | 1 | 0 | | A2, B2 |
| 0 | 1 | 1 | | A3, B3 |
| 1 | X | X | | NONE |
| **CD54/74HC/HCT4053** | | | | |
| **ENABLE** | **S0 or S1 or S2** | | | |
| 0 | 0 | | | A0 or B0 or C0 |
| 0 | 1 | | | A1 or B1 or C1 |
| 1 | X | | | NONE |

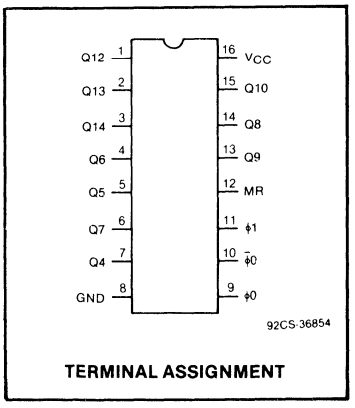
X = Don't care.

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $V_{EE} = 0$V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: A to Output | $C_L$ = 15 pF | 16 | ns |
| | | $C_L$ = 50 pF | 18 | ns |

# CD54/74HC4060
# CD54/74HCT4060

## 14-Stage Binary Ripple Counter with Oscillator




TERMINAL ASSIGNMENT

TRUTH TABLE

| Clock | MR | Output State |
|---|---|---|
| ⌐ | L | No Change |
| ⌐ | L | Advance to next state |
| X | H | All Outputs are low |

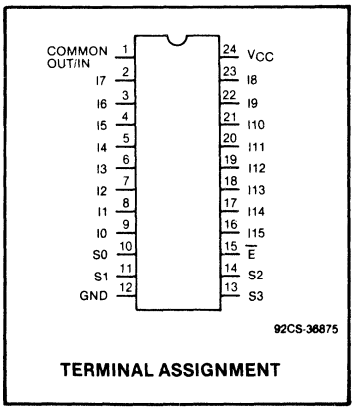
H = high level (steady state)
L = low level (steady state)
X = don't care

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: ϕ0 to $Q_1$ | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC4067
# CD54/74HCT4067

## 16-Channel Analog Multiplexer/ Demultiplexer




TERMINAL ASSIGNMENT

TRUTH TABLE

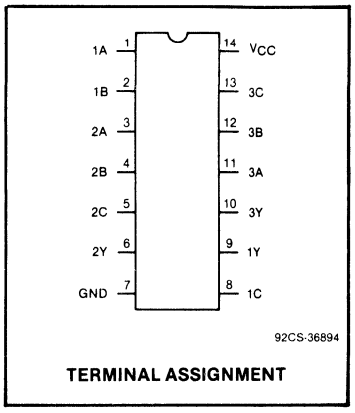
| S0 | S1 | S2 | S3 | E | Selected Channel |
|---|---|---|---|---|---|
| X | X | X | X | 1 | None |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 2 |
| 1 | 1 | 0 | 0 | 0 | 3 |
| 0 | 0 | 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 0 | 0 | 5 |
| 0 | 1 | 1 | 0 | 0 | 6 |
| 1 | 1 | 1 | 0 | 0 | 7 |
| 0 | 0 | 0 | 1 | 0 | 8 |
| 1 | 0 | 0 | 1 | 0 | 9 |
| 0 | 1 | 0 | 1 | 0 | 10 |
| 1 | 1 | 0 | 1 | 0 | 11 |
| 0 | 0 | 1 | 1 | 0 | 12 |
| 1 | 0 | 1 | 1 | 0 | 13 |
| 0 | 1 | 1 | 1 | 0 | 14 |
| 1 | 1 | 1 | 1 | 0 | 15 |

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Address to Output | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 15<br>17 | ns<br>ns |

# CD54/74HC4075
# CD54/74HCT4075

## Triple 3-Input OR Gate



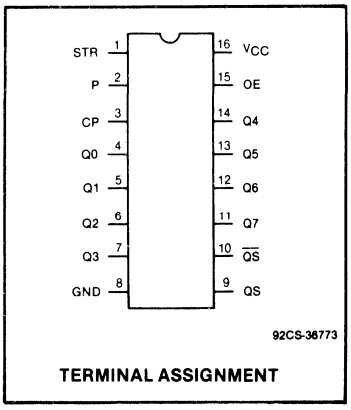

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 10<br>12 | ns<br>ns |

# CD54/74HC4094
# CD54/74HCT4094

## 8-Stage Shift-and-Store Bus Register



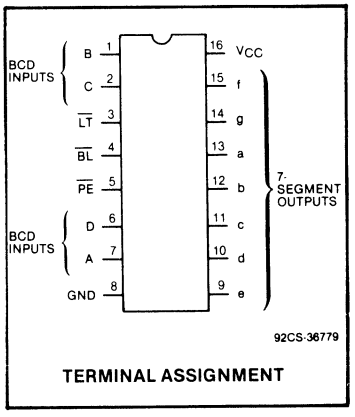

TERMINAL ASSIGNMENT

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC4511
# CD54/74HCT4511

# BCD-To-7 Segment Latch/ Decoder/Driver




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| $\overline{PE}$ | $\overline{BL}$ | $\overline{LT}$ | D | C | B | A | a | b | c | d | e | f | g | Display |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | 0 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| X | 0 | 1 | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 3 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 9 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 1 | 1 | X | X | X | X | | | | * | | | | * |

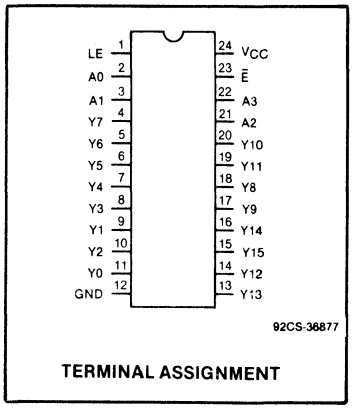
X = Don't Care.
*Depends on BCD code previously applied when $\overline{PE}$ = 0.
Note: Display is blank for all illegal input codes (BCD > 1001).

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output | $C_L$ = 15 pF | 20 | ns |
| | | $C_L$ = 50 pF | 22 | ns |

CD54/74HC4514, CD54/74HCT4514
CD54/74HC4515, CD54/74HCT4515

# 4-to-16 Line Decoder/Demultiplexer with Input Latches




TERMINAL ASSIGNMENT

DECODE TRUTH TABLE (LE = 1)

| ENABLE | DECODER INPUTS | | | | ADDRESSED OUTPUT 4514 = Logic 1 (High) 4515 = Logic 0 (Low) |
|---|---|---|---|---|---|
| | A3 | A2 | A1 | A0 | |
| 0 | 0 | 0 | 0 | 0 | Y0 |
| 0 | 0 | 0 | 0 | 1 | Y1 |
| 0 | 0 | 0 | 1 | 0 | Y2 |
| 0 | 0 | 0 | 1 | 1 | Y3 |
| 0 | 0 | 1 | 0 | 0 | Y4 |
| 0 | 0 | 1 | 0 | 1 | Y5 |
| 0 | 0 | 1 | 1 | 0 | Y6 |
| 0 | 0 | 1 | 1 | 1 | Y7 |
| 0 | 1 | 0 | 0 | 0 | Y8 |
| 0 | 1 | 0 | 0 | 1 | Y9 |
| 0 | 1 | 0 | 1 | 0 | Y10 |
| 0 | 1 | 0 | 1 | 1 | Y11 |
| 0 | 1 | 1 | 0 | 0 | Y12 |
| 0 | 1 | 1 | 0 | 1 | Y13 |
| 0 | 1 | 1 | 1 | 0 | Y14 |
| 0 | 1 | 1 | 1 | 1 | Y15 |
| 1 | X | X | X | X | All Outputs = 0, 4514<br>All Outputs = 1, 4515 |

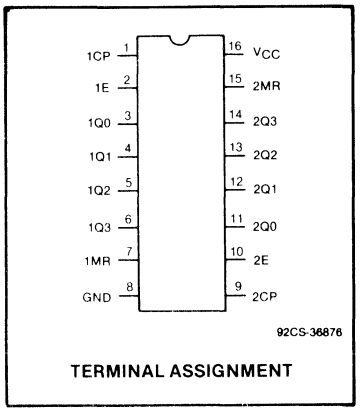
X = Don't Care  Logic 1 = High  Logic 0 = Low

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Data to Output | $C_L$ = 15 pF | 23 | ns |
| | | $C_L$ = 50 pF | 25 | ns |

**CD54/74HC/HCT4518—Dual Synchronous BCD Counters**
**CD54/74HC/HCT 4520—Dual 4-Bit Synchronous Binary Counters**

# Dual Synchronous Counter




TERMINAL ASSIGNMENT

TRUTH TABLE

| CLOCK (CP) | ENABLE (E) | RESET (MR) | ACTION |
|---|---|---|---|
| ⌐‾ | 1 | 0 | Increment Counter |
| 0 | ‾⌐ | 0 | Increment Counter |
| ‾⌐ | X | 0 | No Change |
| X | ⌐‾ | 0 | No Change |
| ⌐‾ | 0 | 0 | No Change |
| 1 | ‾⌐ | 0 | No Change |
| X | X | 1 | Q0 thru Q3 = 0 |

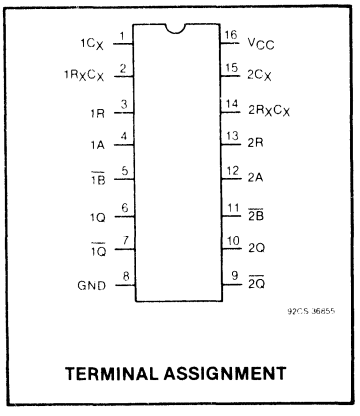
X = Don't Care  1 ≡ High State  0 ≡ Low State

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: CP to $Q_n$ | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 20<br>22 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC4538
# CD54/74HCT4538

# Dual Retriggerable Precision Monostable Multivibrator




TERMINAL ASSIGNMENT

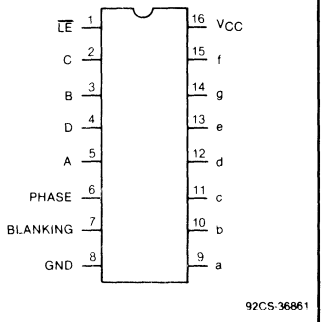
TRUTH TABLE

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Clear | A | B | Q | Q |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↓ | ⎍ | ⎎ |
| H | ↑ | H | ⎍ | ⎎ |

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

# CD54/74HC4543
# CD54/74HCT4543

# BCD-to-7 Segment Latch/ Decoder/Driver for Liquid Crystal Displays




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| INPUT CODE | | | | | | | OUTPUT STATE | | | | | | | DISPLAY CHAR-ACTER |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{LE}$ | Phase | Blank-ing* | D | C | B | A | a | b | c | d | e | f | g | |
| X | 1 | 0 | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 3 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 9 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 0 | 0 | X | X | X | X | ** | | | | | | | ** |
| † | † | 1 | † | | | | Inverse of Output Combinations Above | | | | | | | Display as above |

X = Don't care. † = Above combinations.
* = For liquid-crystal readouts, apply a square wave to PHASE.
For common cathode LED readouts, select PHASE = 0.
For common anode LED readouts, select PHASE = 1.
** = Depends upon the BCD code previously applied when $\overline{LE}$ = 1.

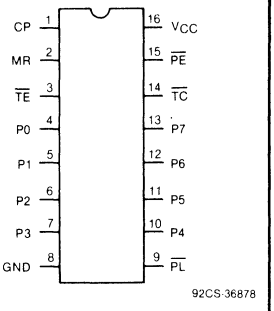
**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Input to Output* | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 18<br>20 | ns<br>ns |

*Standard output only.

## CD54/74HC/HCT40102 — 8-Bit Synchronous BCD Down Counter
## CD54/74HC/HCT40103 — 8-Bit Binary Down Counter

# 8-Bit Down Counter




TERMINAL ASSIGNMENT

**TRUTH TABLE**

| CONTROL INPUTS | | | | PRESET MODE | ACTION |
|---|---|---|---|---|---|
| MR | $\overline{PL}$ | $\overline{PE}$ | $\overline{TE}$ | | |
| 1 | 1 | 1 | 1 | Synchronous | Inhibit counter |
| 1 | 1 | 1 | 0 | | Count Down |
| 1 | 1 | 0 | X | | Preset on next positive clock transition |
| 1 | 0 | X | X | Asynchronous | Preset asynchronously |
| 0 | X | X | X | | Clear to maximum count |

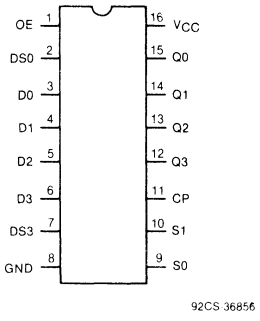
NOTES: 1. 0 = Low level
1 = High level
X = Don't care
2. Clock connected to clock input
3. Synchronous operation: changes occur on negative-to-positive clock transitions
4. P0–P7 inputs: 40102 BCD; MSD = P7, LSD = P0
40103 Binary; MSB = P7, LSB = P0

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: CP to $\overline{TC}$ | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 23<br>25 | ns<br>ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF<br>$C_L$ = 50 pF | 60<br>50 | MHz<br>MHz |

# CD54/74HC40104
# CD54/74HCT40104

## 4-Bit Bidirectional Universal Shift Register, 3-State




TERMINAL ASSIGNMENT

TRUTH TABLE

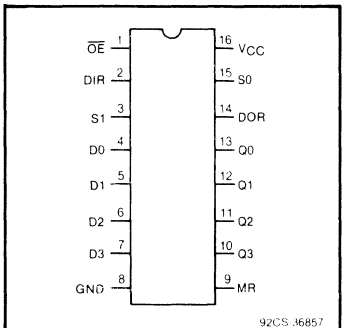
| CP | MODE SELECT $S_0$ | MODE SELECT $S_1$ | OE | ACTION |
|---|---|---|---|---|
| ⎍ | 0 | 0 | 1 | Reset |
| ⎍ | 1 | 0 | 1 | Shift right ($Q_0$ toward $Q_3$) |
| ⎍ | 0 | 1 | 1 | Shift left ($Q_3$ toward $Q_0$) |
| ⎍ | 1 | 1 | 1 | Parallel load |
| X | X | X | 0 | Operations occur as shown above, but outputs assume high impedance |

**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Clock to Output | $C_L = 15$ pF | 18 | ns |
| | | $C_L = 50$ pF | 20 | ns |
| | Enable to HiZ | $C_L = 15$ pF | 12 | ns |
| | Enable from HiZ | $C_L = 50$ pF | 15 | ns |

# CD54/74HC40105
# CD54/74HCT40105

## 4-Bits x 16 Words FIFO Register




TERMINAL ASSIGNMENT

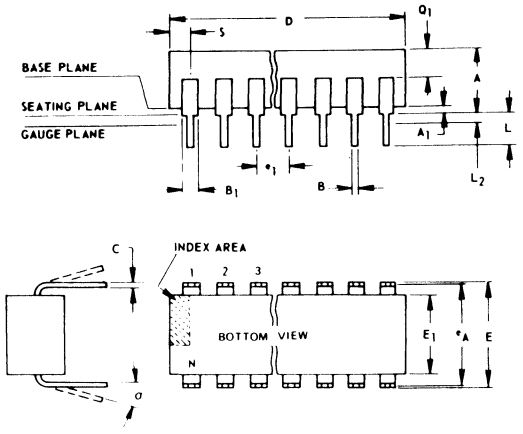
**Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, $t_r$, $t_f = 6$ ns**

| Symbol | Parameter | Test Conditions | Typical | Units |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation Delay: Output Enable to/from HiZ | $C_L$ = 15 pF | 12 | ns |
| | | $C_L$ = 50 pF | 15 | ns |
| | Shift Out to Data Out | $C_L$ = 15 pF | 21 | ns |
| | | $C_L$ = 50 pF | 23 | ns |
| $f_{max}$ | Maximum Clock Frequency | $C_L$ = 15 pF | 60 | MHz |
| | | $C_L$ = 50 pF | 50 | MHz |


# Dimensional Outlines

# Dimensional Outlines

## Dual-In-Line Plastic and Frit-Seal Ceramic Packages




NOTES:

Refer to JEDEC Publication No. 95 for Rules for Dimensioning Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005 " (0.127 mm) radius of True Position (TP) at gauge plane with maximum material condition.
3. $e_A$ applies in zone $L_2$ when unit is installed.
4. Applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. $N_1$ is the quantity of allowable missing leads.

**(E) and (F) SUFFIXES (JEDEC MO-001-AB)**
**14-Lead Dual-In-Line**
**Plastic or Frit-Seal Ceramic Package**

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|---|---|---|---|---|---|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 0.155 | 0.200 | | 3.94 | 5.08 |
| $A_1$ | 0.020 | 0.050 | | 0.51 | 1.27 |
| B | 0.014 | 0.020 | | 0.356 | 0.508 |
| $B_1$ | 0.050 | 0.065 | | 1.27 | 1.65 |
| C | 0.008 | 0.012 | 1 | 0.204 | 0.304 |
| D | 0.745 | 0.770 | | 18.93 | 19.55 |
| E | 0.300 | 0.325 | | 7.62 | 8.25 |
| $E_1$ | 0.240 | 0.260 | | 6.10 | 6.60 |
| $e_1$ | 0.100 TP | | 2 | 2.54 TP | |
| $e_A$ | 0.300 TP | | 2, 3 | 7.62 TP | |
| L | 0.125 | 0.150 | | 3.18 | 3.81 |
| $L_2$ | 0.000 | 0.030 | | 0.000 | 0.76 |
| $\alpha$ | 0° | 15° | 4 | 0° | 15° |
| N | 14 | | 5 | 14 | |
| $N_1$ | 0 | | 6 | 0 | |
| $Q_1$ | 0.040 | 0.075 | | 1.02 | 1.90 |
| S | 0.065 | 0.090 | | 1.66 | 2.28 |

92SS-4296R3

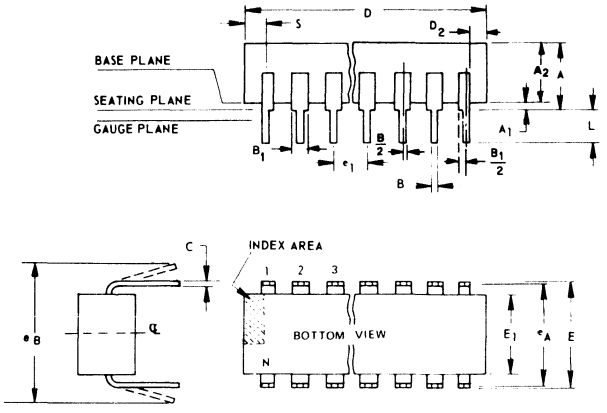
**(E) and (F) SUFFIXES (JEDEC MO-015-AA)**
**24-Lead Dual-In-Line Plastic or**
**Frit-Seal Ceramic Package**

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|---|---|---|---|---|---|
| | MIN. | MAX. | | MIN. | MAX. |
| A | 0.120 | 0.250 | | 3.10 | 6.30 |
| $A_1$ | 0.020 | 0.070 | | 0.51 | 1.77 |
| B | 0.016 | 0.020 | | 0.407 | 0.508 |
| $B_1$ | 0.028 | 0.070 | | 0.72 | 1.77 |
| C | 0.008 | 0.012 | 1 | 0.204 | 0.304 |
| D | 1.20 | 1.29 | | 30.48 | 32.76 |
| E | 0.600 | 0.625 | | 15.24 | 15.87 |
| $E_1$ | 0.515 | 0.580 | | 13.09 | 14.73 |
| $e_1$ | 0.100 TP | | 2 | 2.54 TP | |
| $e_A$ | 0.600 TP | | 2,3 | 15.24 TP | |
| L | 0.100 | 0.200 | | 2.54 | 5.00 |
| $L_2$ | 0.000 | 0.030 | | 0.00 | 0.76 |
| $\alpha$ | 0° | 15° | 4 | 0° | 15° |
| N | 24 | | 5 | 24 | |
| $N_1$ | 0 | | 6 | 0 | |
| $Q_1$ | 0.040 | 0.075 | | 1.02 | 1.90 |
| S | 0.040 | 0.100 | | 1.02 | 2.54 |

92CS26938R3

# Dimensional Outlines

## Dual-In-Line Plastic and Frit-Seal Ceramic Packages




**(E) and (F) SUFFIXES (JEDEC MS-001)**
**16-Lead Dual-In-Line**
**Plastic or Frit-Seal Ceramic Package**

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|---|---|---|---|---|---|
| | MIN. | MAX. | | MIN. | MAX. |
| A | — | 0.210 | 10 | — | 5.33 |
| $A_1$ | 0.015 | — | 10 | 0.39 | — |
| $A_2$ | 0.115 | 0.195 | | 2.93 | 4.95 |
| B | 0.014 | 0.022 | | 0.356 | 0.558 |
| $B_1$ | 0.045 | 0.070 | 3 | 1.15 | 1.77 |
| C | 0.008 | 0.015 | | 0.204 | 0.381 |
| D | 0.745 | 0.840 | 4 | 18.93 | 21.33 |
| $D_2$ | 0.005 | — | 5 | 0.13 | — |
| E | 0.300 | 0.325 | 6 | 7.62 | 8.25 |
| $E_1$ | 0.240 | 0.280 | 7, 8 | 6.10 | 7.11 |
| $e_1$ | 0.090 | 0.110 | 9 | 2.29 | 2.79 |
| $e_A$ | 0.300 TP | | 10 | 7.62 TP | |
| $e_B$ | — | 0.410 | 11 | — | 10.41 |
| L | 0.115 | 0.150 | 10 | 2.93 | 3.81 |
| N | 16 | | 12 | 16 | |
| S | — | — | 13 | — | — |

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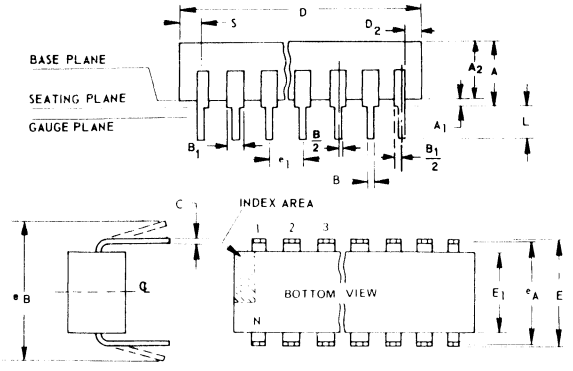
NOTES:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines.
2. Protrusions (flash) on the base plane surface shall not exceed .25 mm (.010 in.).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions 1, N, $\frac{N}{2}$, $\frac{N}{2}$ +1.
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed .25 mm (.010 in.).
5. This dimension is controlling when a particular combination of body length, lead width and lead spacing dimensions would allow lead material to overhang the ends of the package.
6. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
7. Dimension $E_1$ does not include mold flash or protrusions.
8. Package body and leads shall be symmetrical around center line shown in end view within .25 mm (.010 in.).
9. Lead spacing $e_1$ shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
10. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within .25 mm (.010 in.) diameter for dimension $e_A$.
11. $e_B$ is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
12. N is the maximum number of lead positions.
13. Dimension S at the left end of the package must equal dimension S at the right end of the package within .76 mm (.030 in.).

# Dimensional Outlines

## Dual-In-Line Plastic and Frit-Seal Ceramic Packages




NOTES:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines.
2. Protrusions (flash) on the base plane surface shall not exceed .25 mm (.010 in.).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions 1, N, $\frac{N}{2}$, $\frac{N}{2}+1$.
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed .25 mm (.010 in.).
5. This dimension is controlling when a particular combination of body length, lead width and lead spacing dimensions would allow lead material to overhang the ends of the package.
6. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
7. Dimension $E_1$ does not include mold flash or protrusions.
8. Package body and leads shall be symmetrical around center line shown in end view within .25 mm (.010 in.).
9. Lead spacing $e_1$ shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
10. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within .25 mm (.010 in.) diameter for dimension $e_A$.
11. $e_B$ is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
12. N is the maximum number of lead positions.
13. Dimension S at the left end of the package must equal dimension S at the right end of the package within .76 mm (.030 in.).

**(E) SUFFIX**
**20-Lead Dual-In-Line Plastic Package**

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|---|---|---|---|---|---|
| | MIN. | MAX. | | MIN. | MAX. |
| A | — | 0.210 | 10 | — | 5.33 |
| $A_1$ | 0.010 | — | 10 | 0.254 | — |
| $A_2$ | 0.115 | 0.195 | | 2.93 | 4.95 |
| B | 0.014 | 0.022 | | 0.356 | 0.558 |
| $B_1$ | 0.045 | 0.070 | 3 | 1.15 | 1.77 |
| C | 0.008 | 0.015 | | 0.204 | 0.381 |
| D | 0.925 | 1.040 | 4 | 23.49 | 26.42 |
| $D_2$ | 0.005 | — | 5 | 0.13 | — |
| E | 0.300 | 0.325 | 6 | 7.62 | 8.25 |
| $E_1$ | 0.240 | 0.280 | 7, 8 | 6.10 | 7.11 |
| $e_1$ | 0.090 | 0.110 | 9 | 2.29 | 2.79 |
| $e_A$ | 0.300 TP | | 10 | 7.62 TP | |
| $e_B$ | — | 0.410 | 11 | — | 10.41 |
| L | 0.115 | 0.150 | 10 | 2.93 | 3.81 |
| N | 20 | | 12 | 20 | |
| S | — | — | 13 | — | — |

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**(F) SUFFIX**
**20-Lead Dual-In-Line**
**Frit-Seal Ceramic Package**

| SYMBOL | INCHES | | NOTE | MILLIMETERS | |
|---|---|---|---|---|---|
| | MIN. | MAX. | | MIN. | MAX. |
| A | — | 0.210 | 10 | — | 5.33 |
| $A_1$ | 0.015 | — | 10 | 0.39 | — |
| $A_2$ | 0.145 | 0.175 | | 3.68 | 4.44 |
| B | 0.014 | 0.022 | | 0.356 | 0.558 |
| $B_1$ | 0.045 | 0.070 | 3 | 1.15 | 1.77 |
| C | 0.008 | 0.015 | | 0.204 | 0.381 |
| D | 0.942 | 0.990 | 4 | 23.93 | 25.15 |
| $D_2$ | 0.005 | — | 5 | 0.13 | — |
| E | 0.300 | 0.325 | 6 | 7.62 | 8.25 |
| $E_1$ | — | 0.310 | 7, 8 | — | 7.87 |
| $e_1$ | 0.090 | 0.110 | 9 | 2.29 | 2.79 |
| $e_A$ | 0.300 TP | | 10 | 7.62 TP | |
| $e_B$ | — | 0.410 | 11 | — | 10.41 |
| L | 0.115 | 0.150 | 10 | 2.93 | 3.81 |
| N | 20 | | 12 | 20 | |
| S | — | — | 13 | — | — |

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Grand Rapids, MI 49503
**Tel: (616) 243-8805**

**Hamilton Avnet Electronics**
32487 Schoolcraft Road
Livonia, MI 48150
**Tel: (313) 522-4700**

**Schweber Electronics Corp.**
12060 Hubbard Avenue
Livonia, MI 48150
**Tel: (313) 525-8100**

MINNESOTA

**Arrow Electronics, Inc.**
5230 West 73rd Street
Edina, MN 55435
**Tel: (612) 830-1800**

**Hamilton Avnet Electronics**
10300 Bren Road, East
Minnetonka, MN 55343
**Tel: (612) 932-0600**

**Kierulff Electronics, Inc.**
7667 Cahill Road
Edina, MN 55435
**Tel: (612) 941-7500**

**Schweber Electronics Corp.**
7422 Washington Avenue, So.
Eden Prairie, MN 55344
**Tel: (612) 941-5280**

MISSOURI

**Arrow Electronics, Inc.**
2380 Schuetz Road
St. Louis, MO 63141
**Tel: (314) 567-6888**

**Hamilton Avnet Electronics**
13743 Shoreline Court East
Earth City, MO 63045
**Tel: (314) 344-1200**

**Kierulff Electronics, Inc.**
2608 Metro Park Boulevard
Maryland Heights, MO 63043
**Tel: (314) 739-0855**

NEW HAMPSHIRE

**Arrow Electronics, Inc.**
One Perimeter Drive
Manchester, NH 03103
**Tel: (603) 668-6968**

NEW JERSEY

**Arrow Electronics, Inc.**
Pleasant Valley Avenue
Moorestown, NJ 08057
**Tel: (609) 235-1900**

**Arrow Electronics, Inc.**
Two Industrial Road
Fairfield, NJ 07006
**Tel: (201) 575-5300**

**Hamilton Avnet Electronics**
Ten Industrial Road
Fairfield, NJ 07006
**Tel: (201) 575-3390**

**Hamilton Avnet Electronics**
One Keystone Avenue
Cherry Hill, NJ 08003
**Tel: (609) 424-0110**

**Kierulff Electronics, Inc.**
37 Kulick Road
Fairfield, NJ 07006
**Tel: (201) 575-6750**

**Schweber Electronics Corp.**
18 Madison Road
Fairfield, NJ 07006
**Tel: (201) 227-7880**

NEW MEXICO

**Arrow Electronics, Inc.**
2460 Alamo, SE
Albuquerque, NM 87106
**Tel: (505) 243-4566**

**Hamilton Avnet Electronics**
2524 Baylor S.E.
Albuquerque, NM 87106
**Tel: (505) 765-1500**

**Sterling Electronics, Inc.**
3540 Pan American
Freeway, N.E.
Albuquerque, NM 87107
**Tel: (505) 884-1900**

NEW YORK

**Arrow Electronics, Inc.**
20 Oser Avenue
Hauppauge, L.I., NY 11788
**Tel: (516) 231-1000**

**Arrow Electronics, Inc.**
7705 Maltlage Drive
Liverpool, NY 13088
**Tel: (315) 652-1000**

**Arrow Electronics, Inc.**
25 Hub Drive
Melville, LI, NY 11747
**Tel: (516) 391-1640**

**Arrow Electronics, Inc.**
3000 South Winton Road
Rochester, NY 14623
**Tel: (716) 275-0300**

**Hamilton Avnet Electronics**
Five Hub Drive
Melville, L.I., NY 11746
**Tel: (516) 454-6000**

# RCA Authorized Distributors

## U.S. and Canada (Cont'd)

U.S. NEW YORK

**Hamilton Avnet Electronics**
333 Metro Park
Rochester, NY 14623
**Tel: (716) 475-9130**

**Hamilton Avnet Electronics**
16 Corporate Circle
East Syracuse, NY 13057
**Tel: (315) 437-2641**

**Milgray Electronics, Inc.**
191 Hanse Avenue
Freeport, L.I., NY 11520
**Tel: (516) 546-5600**

**Schweber Electronics Corp.**
Three Townline Circle
Rochester, NY 14623
**Tel: (716) 424-2222**

**Schweber Electronics Corp.**
Jericho Turnpike
Westbury, L.I., NY 11590
**Tel: (516) 334-7474**

**Summit Distributors, Inc.**
916 Main Street
Buffalo, NY 14202
**Tel: (716) 884-3450**

NORTH CAROLINA

**Arrow Electronics, Inc.**
5240 Greensdairy Road
Raleigh, NC 27604
**Tel: (919) 876-3132**

**Hamilton Avnet Electronics**
3510 Spring Forest Road
Raleigh, NC 27604
**Tel: (919) 878-0810**

**Kieruliff Electronics Inc.**
1 North Commerce Center
5249 North Boulevard
Raleigh, NC 27604
**Tel: (919) 872-8410**

**Schweber Electronics Corp.**
5285 North Boulevard
Raleigh, NC 27604
**Tel: (919) 876-0000**

OHIO

**Arrow Electronics, Inc.**
7620 McEwen Road
Centerville, OH 45459
**Tel: (513) 435-5563**

**Arrow Electronics, Inc.**
6238 Cochran Road
Solon, OH 44139
**Tel: (216) 248-3990**

**Hamilton Avnet Electronics, Inc.**
4588 Emery Industrial Parkway
Cleveland, OH 44128
**Tel: (216) 831-3500**

**Hamilton Avnet Electronics**
954 Senate Drive
Dayton, OH 45459
**Tel: (513) 433-0610**

**Hughes-Peters, Inc.**
481 East Eleventh Avenue
Columbus, OH 43211
**Tel: (614) 294-5351**

**Kieruliff Electronics, Inc.**
23060 Miles Road
Cleveland, OH 44128
**Tel: (216) 587-6558**

**Schweber Electronics Corp.**
23880 Commerce Park Road
Beachwood, OH 44122
**Tel: (216) 464-2970**

OKLAHOMA

**Kieruliff Electronics, Inc.**
Metro Park 12318 East 60th
Tulsa, OK 74145
**Tel: (918) 252-7537**

OREGON

**Hamilton Avnet Electronics**
6024 S.W. Jean Road,
Bldg. B-Suite J,
Lake Oswego, OR 97034
**Tel: (503) 635-8157**

**Wyle Distribution Group**
5289 N.E. Ezram Young Parkway
Hillsboro, OR 97123
**Tel: (503) 640-6000**

PENNSYLVANIA

**Arrow Electronics, Inc.**
650 Seco Road
Monroeville, PA 15146
**Tel: (412) 856-7000**

**Herbach & Rademan, Inc.**
401 East Erie Avenue
Philadelphia, PA 19134
**Tel: (215) 426-1700**

**Schweber Electronics Corp.**
231 Gibralter Road
Horsham, PA 19044
**Tel: (215) 441-0600**

TEXAS

**Arrow Electronics, Inc.**
13715 Gamma Road
Dallas, TX 75240
**Tel: (214) 386-7500**

**Arrow Electronics, Inc.**
10899 Kinghurst Dr., Suite 100
Houston, TX 77099
**Tel: (713) 530-4700**

**Hamilton Avnet Electronics**
2401 Rutland Drive
Austin, TX 78758
**Tel: (512) 837-8911**

**Hamilton Avnet Electronics**
2111 West Walnut Hill Lane
Irving, TX 75060
**Tel: (214) 659-4111**

**Hamilton Avnet Electronics**
8750 Westpark
Houston, TX 77063
**Tel: (713) 975-3515**

**Kieruliff Electronics, Inc.**
3007 Longhorn Blvd., Suite 105
Austin, TX 78758
**Tel: (512) 835-2090**

**Kieruliff Electronics, Inc.**
9610 Skillman Avenue
Dallas, TX 75243
**Tel: (214) 343-2400**

**Kieruliff Electronics, Inc.**
10415 Landsbury Drive, Suite 210
Houston, TX 77099
**Tel: (713) 530-7030**

**Schweber Electronics Corp.**
4202 Beltway,
Dallas, TX 75234
**Tel: (214) 661-5010**

**Schweber Electronics Corp.**
10625 Richmond Ste. 100
Houston, TX 77042
**Tel: (713) 784-3600**

**Sterling Electronics, Inc.**
2335A Kramer Lane, Suite A
Austin, TX 78758
**Tel: (512) 836-1341**

**Sterling Electronics, Inc.**
11090 Stemmons Freeway
Stemmons at Southwell
Dallas, TX 75229
**Tel: (214) 243-1600**

**Sterling Electronics, Inc.**
4201 Southwest Freeway
Houston, TX 77027
**Tel: (713) 627-9800**

UTAH

**Hamilton Avnet Electronics**
1585 West 2100 South
Salt Lake City, UT 84119
**Tel: (801) 972-2800**

**Kieruliff Electronics, Inc.**
2121 S. 3600 West Street
Salt Lake City, UT 84119
**Tel: (801) 973-6913**

**Wyle Distribution Group**
1959 South 4130 West Unit B
Salt Lake City, UT 84104
**Tel: (801) 974-9953**

WASHINGTON

**Arrow Electronics, Inc.**
14320 N.E. 21st Street
Bellevue, WA 98005
**Tel: (206) 643-4800**

**Hamilton Avnet Electronics**
14212 N.E. 21st Street
Bellevue, WA 98005
**Tel: (206) 453-5874**

**Kieruliff Electronics, Inc.**
1005 Andover Park E.
Tukwila, WA 98188
**Tel: (206) 575-4420**

**Priebe Electronics**
2211 Fifth Avenue
Seattle, WA 98121
**Tel: (206) 682-8242**

**Wyle Distribution Group**
1750 132nd Avenue, N.E.
Bellevue, WA 98005
**Tel: (206) 453-8300**

WISCONSIN

**Arrow Electronics, Inc.**
430 West Rawson Avenue
Oak Creek, WI 53154
**Tel: (414) 764-6600**

**Hamilton Avnet Electronics**
2975 South Moorland Road
New Berlin, WI 53151
**Tel: (414) 784-4510**

**Kieruliff Electronics, Inc.**
2236G West Bluemond Road
Waukesha, WI 53186
**Tel: (414) 784-8160**

**Taylor Electric Company**
1000 W. Donges Bay Road
Mequon, WI 53092
**Tel: (414) 241-4321**

Canada Alberta

**Hamilton Avnet Elec.**
2816 21st St. N.E., Calgary
Alberta, T2E 6Z2
**Tel: (403) 230-3586**

# RCA Authorized Distributors
## U.S. and Canada (Cont'd)

**Canada**

**L. A. Varah, Ltd.**
6420 6A Street SE,
Calgary, Alberta T2H ZB7
**Tel: (403) 255-9550**

**British Columbia**

**L. A. Varah, Ltd.**
2077 Alberta Street,
Vancouver, B.C. V5Y 1C4
**Tel: (604) 873-3211**

**R.A.E. Industrial Electronics, Ltd.**
3455 Gardner Court, Burnaby,
B.C. V5G 4J7
**Tel: (604) 291-8866**

**Manitoba**

**L. A. Varah, Ltd.**
#12 1832 King Edward Street
Winnipeg, Manitoba R2R 0N1
**Tel: (204) 633-6190**

**Ontario**

**Cesco Electronics Ltd.**
24 Martin Ross Road
Downsview, Ontario M3J 2K9
**Tel: (416) 661-0220**

**Electro Sonic, Inc.**
1100 Gordon Baker Road
Willowdale, Ontario M2H 3B3
**Tel: (416) 494-1666**

**Hamilton Avnet (Canada) Ltd.**
6845 Rexwood Drive
Units 3,4,5
Mississauga, Ontario L4V 1M5
**Tel: (416) 677-7432**

**Hamilton Avnet (Canada) Ltd.**
210 Colonnade Street
Nepean, Ontario K2E 7L5
**Tel: (613) 226-1700**

**L. A. Varah, Ltd.**
505 Kenara Avenue, Hamilton,
Ontario L8E 1J8
**Tel: (416) 561-9311**

**Cesco Electronics, Ltd.**
4050 Jean Talon Street, West
Montreal, Quebec H4P 1W1
**Tel: (514) 735-5511**

**Hamilton Avnet (Canada) Ltd.**
2670 Sabourin Street, St.
Laurent, Quebec H4S 1M2
**Tel: (514) 331-6443**

## Europe, Middle East, and Africa

**Austria**

**Transistor Vertriebsgesellschaft MBH & Co KG**
Auhofstrasse 41A,
A-1130 Vienna
**Tel: (02 22)82.94.51/82.94.04**

**Belgium**

**Inelco Belgium S.A.**
Avenue des Croix de Guerre 94
1120 Bruxelles
**Tel: 02/216.01.60**

**Denmark**

**Tage Olsen A/S**
P.O. Box 225
DK - 2750 Ballerup
**Tel: 02/65 81 11**

**Egypt**

**Sakrco Enterprises**
P.O. Box 1133,
37 Kasr El Nil Street, Apt. 5
Cairo
**Tel: 744440**

**Ethiopia**

**General Trading Agency**
P.O. Box 1684
Addis Ababa
**Tel: 132718 137275**

**Finland**

**Telercas OY**
P.O. Box 33
SF - 04201 Kerava
**Tel: 0/248.055**

**France**

**Almex S.A.**
48, rue de l'Aubepine,
F - 92160 - Antony
**Tel: (1) 666 21 12**

**Hybritech**
Avenue de la Baltique
za de Courtaboeuf
F-91940-Les Ulis
**Tel: (6) 928 1000**

**Radio Equipments Antares S.A.**
9, rue Ernest Cognacq,
F - 92301 - Levallois Perret
**Tel: (1) 758 11 11**

**Hybritech**
Avenue de la Baltique
za de Courtaboeuf
F-91940 - Les Ulis
**Tel: (6) 928 1000**

**Tekelec Airtronic S.A.**
Cite des Bruyeres,
Rue Carle Vernet,
F - 92310 - Sevres
**Tel: (1) 534.75.35**

**Germany**

**Alfred Neye Enatechnik GmbH**
Schillerstrasse 14,
2085 Quickborn
West Germany
**Tel: 04106/6120**

**ECS Hilmar Frehsdorf GmbH Electronic Components Service**
Carl-Zeiss Strasse 3
2085 Quickborn
West Germany
**Tel: 04106/71058-59**

**Beck GmbH & Co. Elektronik Bauelemente KG**
Eltersdorfer Strasse 7,
8500 Nurnberg 15
West Germany
**Tel: 0911/34961-66**

**Elkose GmbH**
Bahnhofstrasse 44,
7141 Moglingen
West Germany
**Tel: 07141/4871**

**Sasco GmbH**
Hermann-Oberth-Strasse 16
8011 Putzbrunn bei Munchen
West Germany
**Tel: 089/46111**

**Spoerle Electronic KG**
Max-Planck Strasse 1-3,
6072 Dreieich bei Frankfurt
West Germany
**Tel: 06103/3041**

**Transistor Vertriebsgesellschaft m.b.h. & Co. KG**
Auhofstrasse 41A
A-1130 Vienna
**Tel: (0222) 82.94.51/04**

**Greece**

**Semicon Co.**
104 AeoLou Str.
TT.131 Athens
**Tel: 3253626**

**Holland**

**Vekano BV**
Postbus 6115,
N - 5600 HC Eindhoven
**Tel: (40) 81 09 75**

**Hungary**

**Hungagent**
P.O. Box 542
H-1374 Budapest
**Tel: 01/669-385**

**Iceland**

**Georg Amundason**
P.O. Box 698, Reykjavik
**Tel: 81180**

**Israel**

**Aviv Electronics**
Kehilat Venezia Street 12
69010 Tel-Aviv
**Tel: 03-494450**

**Italy**

**Eledra 3S SpA**
Viale Elvezia 18,
I - 20154, Milano
**Tel: (02) 349751**

**IDAC Elettronica SpA**
Via Verona 8,
I - 35010 Busa di Vigonza
**Tel: (049) 72.56.99**

**LASI Elettronica SpA**
Viale Lombardia 6,
I - 20092 Cinisello
Balsamo (MI)
**Tel: (02) 61.20.441-5**

**Silverstar Ltd.**
Via dei Gracchi 20,
I - 20146 Milano
**Tel: (02) 49.96**

**Morad Yousuf Behbehani**
P.O. Box 146
Kuwait

**Kuwait**

Societe d'Equipement Mecanique et Electrique s.a. (S.E.M.E.)
rue Ibn Batouta 29
Casablanca

**Morocco**

**Tel: (212) 22.08.65**

**National Elektro A/S**
Ulvenveien 75, P.O. Box 53
Okern, Oslo 5
**Tel: (472) 64 49 70**

**Norway**

**Telectra Sarl**
Rua Rodrigo da Fonseca, 103
Lisbon 1
**Tel: 68.60.72-75**

**Portugal**

**Allied Electronic Components (PTY) Ltd.**
P.O. Box 6387
Dunswart 1508
**Tel: (011) 528-661**

**South Africa**

**Kontron S.A.**
Salvatierra 4,
Madrid 34
**Tel: 1/729.11.55**

**Spain**

# RCA Authorized Distributors

## Europe, Middle East, and Africa(Cont'd)

**Spain**

**Novolectric**
Villa roel, 40,
E-Barcelona 11
**Tel: (03) 254.18.07-08**

**Sweden**

**Ferner Electronics AB**
Snormakarvagen 35,
P.O. Box 125,
S-161 26 Bromma Stockholm
**Tel: 08/80 25 40**

**Switzerland**

**Baerlocher AG**
Forrlibuckstrasse 110
8005 Zurich
**Tel: (01) 42.99.00**

**Turkey**

**Teknim Company Ltd.**
Riza Sah Pehlevi Caddesi 7
Kavaklidere Ankara
**Tel: 27.58.00**

**U.K.**

**ACCESS Electronic Components Ltd.**
Austin House, Bridge Street
Hitchin, Hertfordshire SG5 2DE
**Tel: Hitchin (0462) 31 221**

**Gothic Crellon Electronics Ltd.**
380 Bath Road, Slough,
Berks, SL1 6JE
**Tel: Burnham (06286) 4434**

**Jermyn Distribution**
Vestry Industrial Estate
Sevenoaks, Kent
**Tel: Sevenoaks (0732) 450144**

**Macro Marketing Ltd.**
Burnham Lane,
Slough, Berkshire SL1 6LN
**Tel: Burnham (06286) 4422**

**STC Electronic Services**
Edinburgh Way, Harlow
Essex, CM20 2DF
**Tel: Harlow (0279) 26777**

**VSI Electronics (U.K.) Ltd.**
Roydonbury Industrial Park
Horsecroft Road, Harlow
Essex CM19 5 BY
**Tel: Harlow (0279) 29666**

**Yugoslavia**

**Avtotehna**
P.O. Box 593, Celovska 175
Ljubljana 61000
**Tel: 552 341**

**Zambia**

**African Technical Associates Ltd.**
Stand 5196 Luanshya Road
Lusaka

**Zimbabwe**

**BAK Electrical Holdings (Pvt) Ltd.**
P.O. Box 2780
Salisbury

## Asia Pacific

**Australia**

**AWA Microelectronics**
348 Victoria Road
Rydalmere N.S.W. 2116

**Amtron Tyree Pty. Ltd.**
176 Botany Street, Waterloo,
N.S.W. 2017

**Bangladesh**

**Electronic Engineers & Consultants Ltd.**
103 Elephant Road, 1st Floor
Dacca 5

**Hong Kong**

**Gibb Livingston & Co., Ltd.**
77 Leighton Road
Leighton Centre
P.O. Box 55

**Hong Kong Electronic Components Co.**
Flat A Yun Kai Bldg. 1/Fl
466-472 Nathan Road
Kowloon

**India**

Photophone Ltd.
179-5 Second Cross Road
Lower Palace Orchards
Bangalore 560 003

**Indonesia**

**NVPD Soedarpo Corp.**
Samudera Indonesia Building
JL Letten, Jen. S
Parman No. 35 Slipi
Jakarta Barat

**Japan**

**Okura & Company Ltd.**
3-6 Ginza, Nichome, Chuo-Ku
Tokyo 104

**Korea**

**Panwest Company, Ltd.**
C.P.O. Box 3358
Room 603, Sam Duk Building
131, Da-Dong, Chung-Ku
Seoul, Republic of South Korea

**Nepal**

**Continental Commercial Distributors**
Durbar Marg.
Kathmandu

**New Zealand**

**AWA NZ Ltd.**
N.Z. P.O. Box 50-248
Porirua

**Philippines**

**Philippine Electronics Inc.**
P.O. Box 498
3rd Floor, Rose
Industrial Bldg., 11 Pioneer St.
Pasig, Metro Manila

**Semitronics Philippines**
216 Ortego Street
San Juan 3134, Metro Manila

**Singapore**

**Device Electronics Pte. Ltd.**
101 Kitchener Road No. 02-04
Singapore 0820

**Microtronics Asso. Pte. Ltd.**
Block 1003, Unit 35B
Aljunied Avenue 5
Singapore 1438

**Sri Lanka**

C.W. Mackie & Co. Ltd.
36 D.R. Wijewardena Mawatha
Colombo 10

**Taiwan**

**Delta Engineering Ltd.**
No. 42 Hsu Chang Street
8th Floor, Taipei

**Multitech International Corp.**
No. 315, Fu Shing North Road
Taipei

**Thailand**

**Anglo Thai Engineering Ltd.**
2160 Ramkambaeng Road
Highway Hua Mark, Bangkok

**Better Pro Co. Ltd.**
71 Chakkawat Road
Wat Tuk, Bangkok

## Latin America

**Argentina**

**Eneka S.A.I.C.F.I.**
Tucuman 299,
1049 Buenos Aires
**Tel: 31-3363**

**Radiocom S.A.**
Conesa 1003,
1426 Buenos Aires
**Tel: 551-2780**

**Tecnos S.R.L.**
Independencia 1861
1225 Buenos Aires
**Tel: 37-0239**

**Brazil**

**Commercial Bezerra Ltda.**
Rua Costa Azevedo, 139,
CEP-69.000 Manaus/AM
**Tel: (092) 232-5363**

**Panamericana Comercial Importadora Ltda.**
Rua Aurora, 263,
01209, Sao Paulo, SP
**Tel: (011) 222-3211**

**Chile**

**Raylex Ltda.**
Av Providencia 1244,
Depto.D, 3er Piso
Casilla 13373, Santiago
**Tel: 749835**

**Industria de Radio y Television S.A. (IRT)**
Vic. MacKenna 3333
Casilla 170-D, Santiago
**Tel: 561667**

**Colombia**

**Miguel Antonio Pena Pena Y Cia. S. En C.**
Carrera 12 #1906
Bogota

**Electronica Moderna**
Carrera 9A, NRO 19-52
Apartado Aereo 5361
Bogota, D.E.1

**Costa Rica**

**J. G. Valldeperas, S.A.**
Calle 1, Avenidas 1-3,
Apartado Postal 3923
San Jose
**Tel: 32-36-14**

**Dominican Republic**

**Humberto Garcia, C. por A.**
El Conde 366
Apartado de Correos 771
Santo Domingo
**Tel: 682-3645**

# RCA Authorized Distributors
## Latin America (Cont'd)

**Ecuador**

**Elecom, S.A.**
Padre Solano 202-OF. 8,
P.O. Box 9611, Guayaquil

**El Salvador**

Radio Electrica, S.A.
4A Avenida Sur Nb. 228
San Salvador
**Tel: 21-5609**

**Radio Parts, S.A.**
2A C. O. No. 319 Postal la
Dalia, P.O. Box 1262
San Salvador
**Tel: 21-3019**

**Guatemala**

**Electronics Guatemalteca**
13 Calle 5-59, Zona 1
P.O. Box 514
Guatemala City
**Tel: 25-649**

**Tele-Equipos, S.A.**
10A Calle 5-40, Zona 1
Apartado Postal 1798
Guatemala City
**Tel: 29-805**

**Haiti**

**Societe Haitienne D'Automobiles, S.A.**
P.O. Box 428,
Port-Au-Prince
**Tel: 2-2347**

**Honduras**

**Francisco J. Yones**
3A Avenida S.O. 5
San Pedro Sula,
Honduras, Central America
**Tel: 52-00-10**

**Mexico**

**Electronica Remberg, S.A. de C.V.**
Republica del Salvador No.
30-102, Mexico City 1, D.F.
**Tel: 510-47-49**

**Mexicana de Bulbos, S.A.**
Michoacan No. 30
Mexico 11, D.F.
**Tel: 564-92-33**

**Partes Electronicas, S.A.**
Republica Del Salvador 30-501
Mexico City
**Tel: (905) 585-3640**

**Raytel, S.A.**
Sullivan 47 Y 49
Mexico 4, D.F.
**Tel: 566-67-86**

**Netherland Antilles**

**El Louvre, S.A.**
P.O. Box 138, Curacao
**Tel: 54004**

**Nicaragua**

**Comercial F. A. Mendieta, S.A.**
Apartado Postal No. 1956
C.S.T. 5c Al Sur 2c 1/2 Abajo
Managua

**Panama**

**Tropelco, S.A.**
Via Espana 20-18, Panama 7
Rep. de Panama

**Paraguay**

**Compania Comercial Del Paraguay, S.A.**
Casilla de Correo 344
Chile 877, Asuncion

**Peru**

**Arven S.A.**
PSJ Adan Mejia 103, OF. 33
Lima 11
**Tel: 716229**

**Surinam**

**Kirpalani's Ltd.**
17-27 Maagdenstreet,
P.O. Box 251, Paramaribo
**Tel: 71-400**

**Surinam Electronics**
Keizerstreet 206
P.O. Box 412
Paramaribo
**Tel: 76-555**

**Trinidad**

**Kirpalani's Limited**
Kirpalani's Komplex
Churchill Roosevelt Highway
San Juan, Port-of-Spain
**Tel: 638-2224/9**

**Uruguay**

**American Products S.A. (APSA)**
Casilla de Correo 1438
Canelones 1133
Montevideo
**Tel: 594210**

**Venezuela**

**P. Benavides, P., S.R.L.**
Residencies Camarat, Local 7
La Candelaria, Caracas
MAIL ADDRESS: Apartado Postal 20.249
San Martin, Caracas
**Tel: (58-2) 571-21-46**

**West Indies**

**Da Costa and Musson Ltda.**
Carlisle House
Hincks Street
P.O. Box 103
Bridgetown, Barbados
**Tel: 608-50**

RCA Solid State

# DATABOOK